SIEMENS

ISDN So Analyzer

K1403

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Kommunikationsmeßtechnik

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ISDN S_0 ANALYSER K1403

Notices to the Software V 4.0

Functional Tests

- Entry of Testsuite Parameters for „TTCN“ Tests Appendix B2 via IEC bus
  - You have to enter the „test suite parameters“ in the menu „TTCN“ Tests Appendix B1. Afterwards „Start“ and „stop“ this measurement. Now the „test suite parameters“ for the „TTCN“ Tests Appendix B2 are installed.

Jitter Option:

- Jitter measurement NT
  - The selected load (25 mW, 380 mW, ...) is not connected to the IUT (NT)
- Jitter measurement TE
  - After stopping the Jitter measurement with Jitter generator „ON“ and „continuous 0 or continuous 1“ there is put out an error message „time out start again“. This is a faulty error message.

Parameters for Menu and IEC:

Parameter errors (lines with errors are underlined)

page: 7-39; chapter: 7.5.5 Short interruption

No.	Meaning	Comments
10	Control 0: external voltage dips manual 1: internal voltage dips manual 2: internal voltage dips automatical	only permitted, if par. no. 1 = 0; otherwise set par. no.10 = 0

page: 7-42; chapter: 7.6.1 Normal/restricted: power output

No.	Meaning	Comments
2	Minimum voltage (PS1) in steps of 1 V Range: 6-56 (6V - 56V)	Only effective if par. no. 1 = 0
3	Minimum voltage (PS2) in steps of 1 V Range: 6-56 (6 V - 56 V)	Only effective if par. no. 1 = 1
4	Maximum load current in steps of 0.25 mA Range: 4-1200 (1 - 300 mA)	
6	Current change delta I in steps of 0.25 mA Range: 1-80 (0,25 - 20 mA)	

page: 7-43; chapter: 7.6.2 Normal/restricted: switchover test

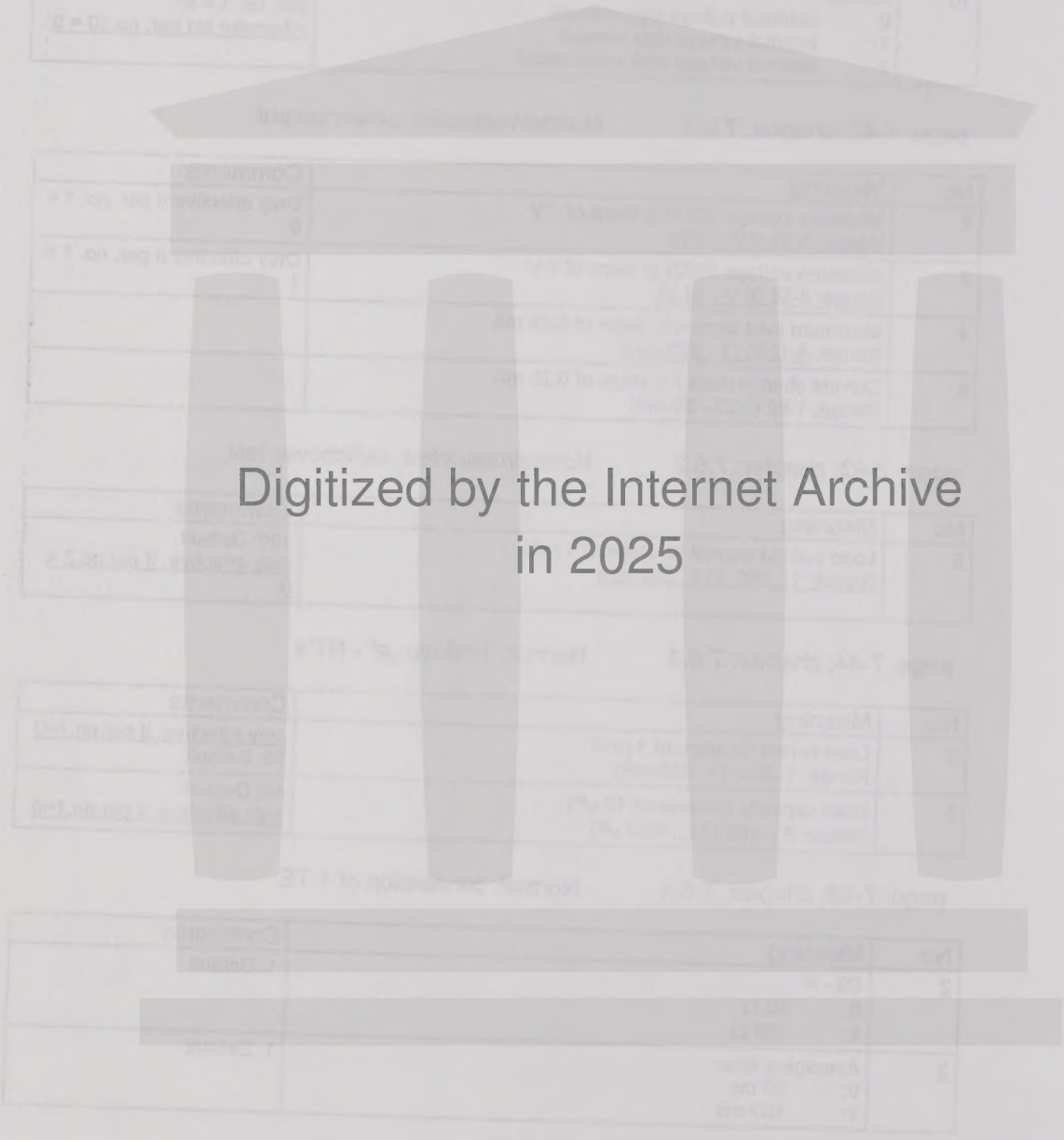
No.	Meaning	Comments
3	Load current normal (in steps of 1 mA) Range: 11..300 (11...300 mA)	100: Default only effective, if par.no.2 = 0

page: 7-44; chapter: 7.6.3 Normal: Test typ „a“ - NT's

No.	Meaning	Comments
2	Load curent (in steps of 1 mA) Range: 1..300 (1...300 mA)	only effective, if par.no.1=0 60: Default
3	Load capacity (in steps of 10 µF) Range: 5....100 (50...1000 µF)	40: Default only effective, if par.no.1=0

page: 7-45; chapter: 7.6.4 Normal: connection of 1 TE

No.	Meaning	Comments
2	S0 - R 0: 50 Ω 1: 100 Ω	1: Default
3	Averaging time 0: 50 ms 1: 100 ms	1: Default



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page: 7-47; chapter: 7.6.9 Restricted (D): following capacitive short circuit

No.	Meaning	Comments
2	Load capacity (in steps of 10 µF) Range: 5....100 (50...1000 µF)	10: Default (only effective if par no. 1 = 0)

page: 7-49; chapter: 7.6.10 Jitter TE

No.	Meaning	Comments
12	Jitter magnitude 2: 0.008 / 0.004 UIpp 3: 0.012 / 0.006 UIpp 4: 0.016 / 0.008 UIpp ..... 175: 0.700 / 0.350 UIpp	Dependant on par. no. 11 Only effective if par. no. 13 = 1

page:7-50 and 7-51; chapter: 7.6.11 Jitter NT

No.	Meaning	Comments
2	Transmitted data 0: 'Binary 1' 1: 'Binary 0' 2: 'Alternating Pattern' 3: 2 EXP 9 -1 4: 2 EXP 11-1 5: 2 EXP 15-1 6: 2 EXP 19-1 7: Extern B1 8: Extern B1 + B2	
11	DEFAULT: 0	set par.no.11=0
12	Clock 0: 15.36 Mhz 1: 12.288 MHz	

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C73000–X6076–C53–4

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The product described in this manual complies with the statutory regulations on electromagnetic compatibility of devices (EMC) or the regulations of the guideline of the council from 03.05.1989 for adaptation of the statutory regulations of the member countries on electromagnetic compatibility of devices (89/336/EEC).

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ISDN S_0 Analyzer K1403

Version 4.00

User Manual C73000-B6076-C153-4

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1 About K1403

The ISDN S_0 Analyzer K1403 is a measuring station which can be used to perform measurements on the S_0 bus. Its compact design means it can be used equally well for R&D, testing and maintenance.

The K1403 provides a number of tests that are defined in accordance with the CCITT I.430, ETSI 300 012, FTZ 1TR3 and NET3 guidelines. Its modular design means it can be expanded and thus easily adapted to special measuring tasks.

ISDN S_0 Analyzer K1403 is a compact test set which combines in a single unit all the modules, signals, auxiliary signals and analyzers required for performing measurement tasks.

Design and mode of operation

ISDN S_0 Analyzer K1403 has a powerful processor for coordinating the functions of the individual modules. Each module is controlled by its own microprocessor and performs a number of measurement tasks. The unit has a large electroluminescent (EL) display for displaying the results in either graphic or alphanumeric form, complete with all important measurement parameters. The active area is approx. 100 x 200 mm large and consists of 256 x 512 image points.

The analyzer is operated very simply by means of an infrared touch panel. The display only shows the keys which are required for any given operation. The keys are actuated by simply touching them. A total of 16 x 32 IR light barriers form a matrix of 512 very small contact fields which can be combined into large touch areas to suit the particular application. The touch panel functions can be disabled e.g. for continuous measurements by means of a special PADS LOCK key T6.

Menu operation of the unit is divided into two, very well arranged input levels. Functions or parameters can be changed very easily using selection windows.

The K1403 is fitted with a complete synthesizer which, with a favourable ratio of spurious-to-wanted signal, enables the necessary sinusoidal signals to be generated under crystal control over the range from 2 kHz to 1 MHz.

The receiver in the K1403 functions selectively. The bandwidth of 25 Hz is produced by means of a mechanical filter. The test modules are connected to the test object by means of a measuring panel by selecting the measuring mode in the parameter menu. The measuring panel includes a relay switching panel, all reference test objects and precision transformers.

A digital storage oscilloscope, a high-frequency counter and various test pattern generators and detectors are also integrated in a module for performing further analog measurements.

Power feeding conditions and the external feed of the test object are measured by another module which is also controlled by a local microcomputer.

The results are evaluated so that they require no further processing by the user. The results are presented in a graphical display, either with or without tolerance lines. The following table "Measuring modes" shows the measurements which can be performed with ISDN S0 Analyzer K1403.

Measuring modes K1403

Measuring mode	Test object	
	TE	NT
• **Electrical characteristics**		
Impedance	+	+
Impedance of active transmitter	+	+
Unbalance	+	+
Peak output current	+	+
Clock accuracy	+	n.d.
Pulse shape	+	+
Pulse unbalance	+	n.d.
Frame delay	+	n.d.
Output jitter	+	+
• **Power feeding conditions**		
Power consumption/output	+	+
Current/time conditions	+	-
Power start-up test	+	-
Switch on/off tests	+	+
Overload tests	-	+
Load change test	-	+
• **Options**		
a) S_0 artificial line	+	+
b) Jitter	+	+
c) Functional tests		
Receiver sensitivity (contained in option c)	+	+

n.d.: non-defined measuring mode

No additional test units are required for the above measuring modes. Only when measurements are performed at the active network termination (NT) is the ISDN NT test set K1400 required for simulating the LT functions of the digital exchange.

All the important functions on the ISDN S_0 Analyzer can be remote-controlled via the IEC bus (IEEE 488.2).

1.1 About this manual

The present user manual contains a description of the ISDN S0 Analyzer K1403 as well as operating instructions for this device. Knowledge of the technical applications is prerequisite.

The introductory section, which you are reading at present, introduces the most important features of K1403. Please be sure to note the safety information at the end of this introduction!

Section 2, "Device description", describes the hardware of the K1403. In section 3, "Start-up preparations", you will learn how to make the K1403 ready for use. Chapter 4, "Operation", introduces the operating unit of the K1403.

Chapter 5 will introduce you to the various measurement modes possible with the K1403: For each measurement, the parameter settings, the measurement method and the result representation are described.

In Chapter 6, "Remote control of the K1403", you will be informed on how to remotely control the K1403 with commands.

Chapter 7 and 8 will give you an overview of the "Menu and IEC parameters", as well as the "Result structures" for each measuring mode K1403.

In the "Appendix" you will find the technical data for the K1403. Installation of the V.24 printer interface is also described here. You are also provided with information on care and maintenance and our service offer.

The present manual uses the following **graphical conventions**:

"Messages"
from the system are given in quotes.

`Font Courier`
indicates menus, commands and parameters.

The arrow head (➤)
indicates instructions which are to be carried out.

Furthermore, the following symbols are used in the manual:

Additional information.
This information may be useful to you.

Warning!
This note is for your own safety and must be observed.

1.2 Safety information

The ISDN S_0 Analyzer K1403 has been constructed and tested in accordance with Publication EN61010 Safety Provisions for Electronic Measuring Equipment, and has left the factory in a perfectly safe condition. In order to maintain optimum safety and ensure hazard-free operation, please adhere to the following basic rules.

- Transport the device only in its original packing or by using the transport case specially recommended for the K1403. This will protect the device against shocks.
- The K1403 is exclusively intended for indoor use. Condensation may occur when the unit is brought to its site of operation from a cold environment. Operation is only permissible with an absolutely dry unit after its temperature has adjusted to the environment.
- Before implementing and operating the K1403, make sure that the environmental conditions are complied with. The environmental conditions are listed under the heading "Technical data" in the appendix.
- Before switching on the device, make sure that the preset operating voltage of the device corresponds to the permissible line voltage.
- Make sure that replacement fuses are of the specified type and rating: Use 3.15A/250 V (type T) fuses.
- The power plug must only be inserted into a grounded socket. Do not cancel the protective effect by using an extension cable without a protective ground conductor.
- Make sure that the ventilation slots on the rear and top of the device are not covered.
- The unit can become dangerous if the protective ground conductor is interrupted either inside or outside the unit. Do not interrupt the protective ground conductor intentionally. The same applies when loosening the connection for the protective ground conductor. When opening covers or removing parts, remember that live parts may be exposed if the unit is connected. Connection points may also be live. Disconnect the unit from all voltage sources prior to adjustment, maintenance, repair or when replacing modules and parts. If such work on live and open units cannot be avoided, it should only be performed by qualified staff familiar with the hazard involved.
- All modules contain electro-sensitive components. Please note the necessary precautions and ESD safety measures.

Warning!

When electrical devices are in operation certain parts of these device are live. Non-observance of the above precautions may therefore lead to severe physical injuries or to serious material damage.

Only qualified staff may handle this device or work in its vicinity. They must be thoroughly familiar with all the warnings, safety and maintenance information contained in these instructions. Faultless and safe operation of the device presupposes proper transport, proper storage, set-up and mounting as well as careful handling and servicing.

2 Device description

The **interconnection board** of the K1403 contains all the slots for the individual printed circuit boards. The slots are electrically identical, apart from that for the CPU. However, the printed circuit boards are fitted as outlined below (cf. rear panel designation strip).

Measuring panel	C73249-A11-L11	Slot	1	
Analog1	C73249-A11-L8/L80	"	2	Option
Analog2	C73249-A11-L91	"	3	Option
Jitter	C73249-A11-L30	"	4	Option
Functional tests	C73249-A11-L15	"	5	
Artificial line	C73249-A11-L160	"	6	Option
Power feeding condition	C73249-A11-L100	"	7	
CPU	C73249-A11-L12	"	8	

The *Power Board* C73249-A11-L101 is fitted in addition on the protective panel of the AC line adapter and connected to the -L100 by a ribbon cable and a multi-core, twisted cable.

The interconnection board also contains the internal connections for the AC line adapter as well as test sockets BU1 to BU 7.

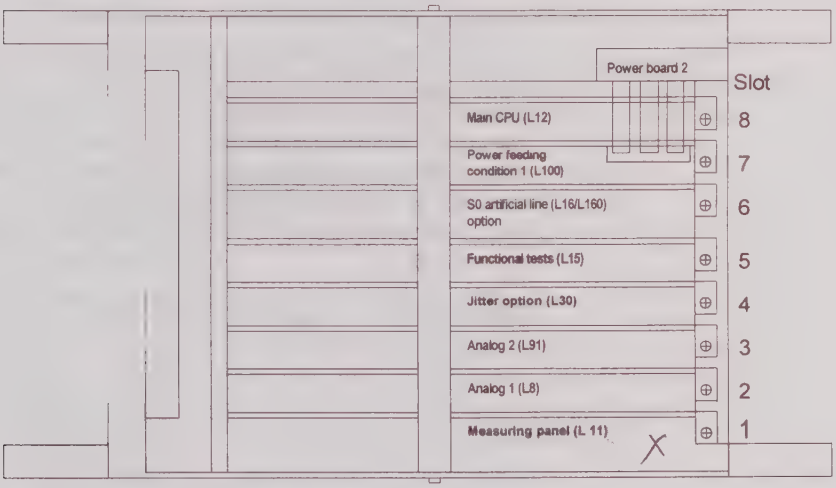


Fig. 2.1: K1403 interior view

2.1 Power feeding conditions

This unit measures the feeding characteristics of ISDN terminal equipment TE or a network terminator NT in accordance with guideline FTZ-1TR211 of the German Postal Services and the international guideline ETSI 300_012. The measurements are made on the floating, balanced-to-earth TE power supply or the NT source. For this reason, the module computer and all test components are floating.

The test unit consists of two modules, the power-generating unit (L101) and the actual test module (L100).

Power module L101

The power module consists of the following components (cf. block diagram)

- Low-pass filter and amplifier
- Power amplifier
- Transformer
- Voltage sources U1 + U2
- Current sink
- Power supply L100
- Drive and control

A square-wave signal with a low frequency (17 kHz) is obtained from the processor clock and applied to a power amplifier following amplification and filtering. The power amplifier is connected as a push-pull stage and delivers the primary current required for the transformer. Its gain is fixed internally to 20 dB. The various voltages are derived on the secondary side of the transformer (S_0 basic voltage, supply voltages for the floating circuit components). The S_0 basic voltage is connected to the actual test module L100 via two controllable voltage sources and a controllable current sink.

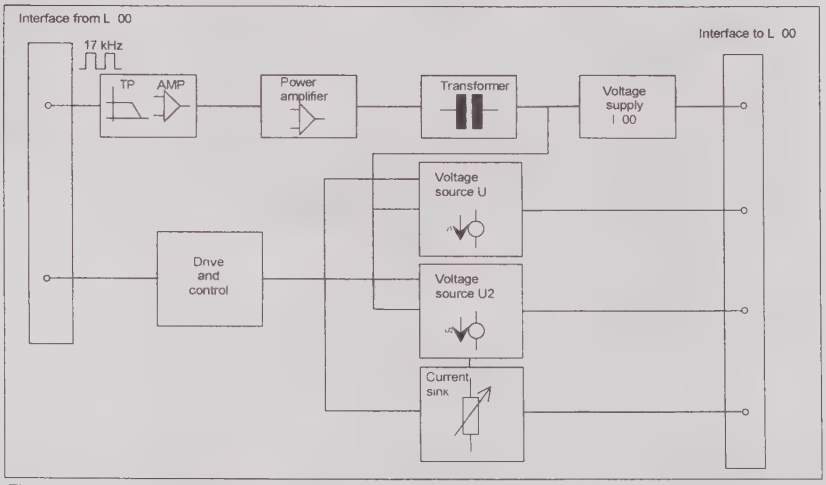


Fig. 2.2: Power feeding module (L101)

Test module L100

The test module L100 consists of the following components (cf. block diagram)

- Measuring and relay panels
- Input amplifier
- A/D converter
- Controller
- Trigger circuit
- Transient recorder
- CPU
- FIFO interface

The test unit "Power feeding conditions" (L100 + L101) is used for the following measuring modes:

- Power consumption on the TE
- Current/transient measurement on the TE
- Current/time measurement on the TE
- Start-up and interruption tests on the TE
- Switchover from normal mode to restricted mode and vice versa on the TE
- Power output of NT
- Switchover from normal mode to restricted mode on the NT
- Connection of TE to NT
- Switching on of NT
- Short circuit on the NT

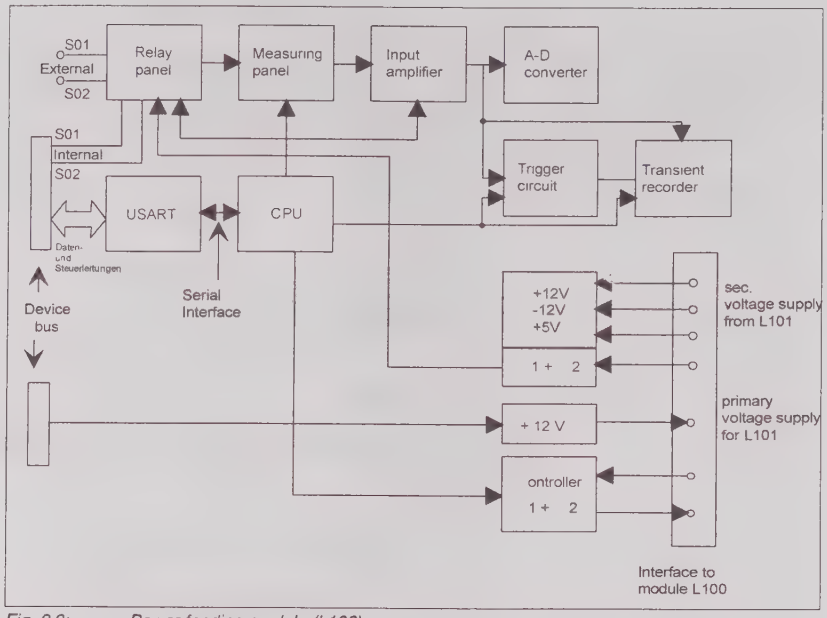


Fig. 2.3: Power feeding module (L100)

The measuring and relay panels

The voltage paths of the two voltage sources required for the supply and measurement of the S_0 interface are combined on the relay panel. Bistable and monostable relays are used. The relays are activated via the module computer.

On the measuring panel, the ranges for current measurement/limitation are set by the connection/parallel connection of various precision resistors. Various series resistors can be connected in addition. The measuring paths are switched through by relays, the coupling to the instrument amplifiers is made via FET switches.

The input amplifier

The input amplifier consists of two operational amplifiers with programmable gains. The measured variables are connected to the input amplifier via FET multiplexers. An operational amplifier with a fixed gain is additionally present to decouple the input amplifier from the following 12-bit A/D converter.

The following relationship results from the precision resistors of the measuring panel and the programmable gains of the input amplifier.

Calculation of current measuring ranges

$$I_{max} = \frac{U_{ref}}{R_M}(V * V_1 * V_2)$$

where

I_{MAX}	:	Maximum current
U_{REF}	:	Reference for ADC: 3 V
R_M	:	Precision resistor
V	:	Gain of input amplifier (V4)
V_1	:	Gain of first operational amplifier AD526
V_2	:	Gain of second operational amplifier AD526

1Ω current measuring range

R_M : 1Ω //1000Ω (the resistance is slightly larger in practice since the voltage drop across the conductor path must be taken into consideration)

V1 = 2	**V2 = 1**	**I_{max} = 375 mA**

5Ω current measuring range

R_M : Precision resistor: 4.9261Ω (because of parallel connection of 1000Ω resistor)

V1 = 4	**V2 = 1**	**I_{max} = 38 mA**

15Ω current measuring range

R_M : Precision resistor: 15Ω

V1 = 8	**V2 = 1**	**I_{max} = 6.25 mA**

1000Ω current measuring range

R_M : Precision resistor: 1000Ω

V1 = 1	**V2 = 1**	**I_{max} = 750 µA**

The inputs are protected against overvoltages by protective diodes.

A/D converter

A 12-bit converter with a max. sampling rate of 10 kHz (as a result of CPU cycle times) and an input voltage window of ± 3 V is used as the A/D converter. It is used to digitize the measured signals, e.g. the current and voltage from test objects or internal signal variables, and processed further by the CPU.

Regulation

Two regulated voltage sources and one regulated current sink are present on the power module L101. Part of this control is present on the module L100. The voltage (current) to be controlled is determined via the instrument amplifier and A/D converter, the controlled variable calculated from this and put via control elements into the control loop.

Trigger circuit

This circuit component is part of the transient recorder. Depending on the selected trigger mode, it is used to switch the trigger paths and to generate the trigger signal for the transient recorder via a comparator. Gradient triggering (change in current with respect to time) as well as level triggering are possible with this circuit.

Transient recorder

The module contains a transient recorder to measure fast dynamic processes. It can be used to measure non-recurring events (transients) by means of an 8-bit A/D converter with a max. sampling rate of 20 MHz and a memory depth of 4 K.

CPU

An Intel processor of type 80C32 is used. This CPU controls the relay panel, measuring panel, input amplifier, trigger circuit and transient recorder. It evaluates the results, processes them and applies the result via the built-in serial interface to the main computer. The main computer passes on the information required for the respective measurement to the module computer via the same interface. The serial interface of the CPU can also be used directly for test purposes.

Serial interface

The parallel data bus (D0 to 7) with the control lines (/RD, /WR, /CS, A1) of the main computer is connected to the USART module. The clock for the serial interface is generated by an oscillator/divider. The required transmission rate can be set using jumpers.

X220 = 9600 Bd

X221 = 4800 Bd

X222 = 2400 Bd

X223 = 1200 Bd

The optocouplers provide electrical isolation between the main computer and the module computer.

2.2 Measuring panel

The module "MEASURING PANEL" consists of the following circuit components:

- Relay panel and its controller
- Balance bridge
- Impedance bridge
- DC unbalance
- S_0 transformers
- Resistance network
- TE load
- Isolated unity-gain amplifier
- S_0 bus voltage detector
- Reference

The relay panel and its controller

The relay panel consists of 30 monostable relays, each with 4 NO contacts (S4-5V), or 2 NO contacts and 2 NC contacts (S2-5V). They show good RF characteristics through their high crosstalk attenuation of at least 74 dB at 1 MHz and low contact capacitances. The relay's most important characteristic data are as follows:

Coil voltage	5 V
Contact/through resistance	20/30 mΩ
Contact capacitance	< 1.5 pF
Operate/bounce time	10 /2 ms
Coil resistance	130 Ω

The relay coils are controlled via a 4 x 7-fold Darlington transistor array which can drive up to 500 mA in each case. The controlling registers are set by two 16-bit data words.

The module version number can be read from one of these registers in the least significant 4 data bits D3 to D0. The coding is set with 4 pairs of resistors.

The measuring panel is addressed by the host by two addresses:

H address : "0001H"

L address : "0000H"

The relay arrangements for the respective address are as follows:

Data "H"

XX 29/30 28 27	25 24 23 22	XX 21 20 19	18 17 16 15

Data "L"

XX 14 13 12	11 10 09 08	XX 07 06 05	04 03 02 01

XX represents the bits for the self test.

Balance bridge

The balance bridge allows LCL measurements. It contains all the components required by CCITT I.430.

T1 and T2 are symmetrical transformers whose intrinsic longitudinal balance at f < 300 kHz exceeds 74 dB.

Chokes L1 and L2 are used for AC isolation of the balance bridge from the power supply. They have an inductance of L > 50 mH.

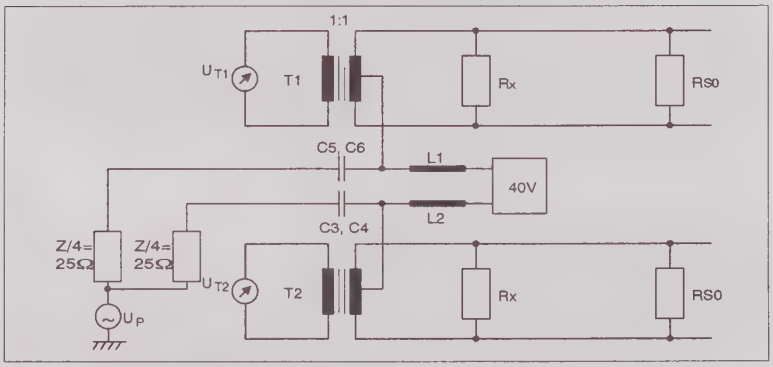


Fig. 2.4: Balance bridge

The Z/4 impedances are implemented by groups of resistors. They are connected to the symmetrical transformers T1 and T2 via C3, C4 and C5, C6 respectively. R = Rx || R_{S0} = 100 Ω || 100 Ω = 50 Ω is switched on the module for an S_0 bus load. This means that the test object must not contain a terminating resitor TR = 100 Ω in the case of unbalance measurement. (The result is approx. 3 dB higher with the terminating resistor switched on than the unbalance values without terminator).

Warning!

When using measuring mode "Earth unbalance" (longitudinal balance, LCL), isolation of the electrical ground and protective earth is cancelled for test purposes. The maximum permissible isolation voltage between test sockets BU6 and protective earth and between BU7 and protective earth is 100 V.

When using a non-isolated IEC bus card, the electrical isolation of device-internal ground and protective ground is also cancelled.

Impedance bridge

The impedance bridge is used for performing various impedance measurements between 2 kHz and 1 MHz. It consists of two precision transformers and a current transformer.

The precision transformers are symmetrical 1:1 transformers and are used for DC isolation. The current transformer is designed as a Marconi transformer and is used for the current measurement. The DC component from the two windings pin 4 → pin 5 and pin 10 → pin 9 is cancelled out by the same number of turns and the opposed winding direction. The AC component, however, is amplified approx. 6 times and is available as an output voltage between pin 2 and pin 7. The AC impedance on the primary side is < 5 Ω per line and is identical on both S_0 lines.

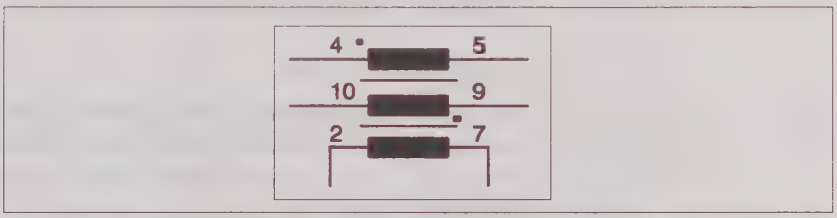


Fig. 2.5: Impedance bridge

S0 transformers

The S_0 transformers used on the measuring panel are 1:1 transformers capable of being loaded with a DC unbalance of at least 3 %.

They are used during the functional tests. Isolation of the unity-gain amplifier of the transmitted level stabilizer (AGC) is attained during impedance measurement using a further transformer.

Resistance network

The various S_0 impedances are switched on/off by the resistance network depending on the measuring mode. The impedances on the various pairs of lines can be adjusted independently of one another and can be connected to each pair of lines on the test object in order to perform measurements on the TE or NT side as required.

The Z-values which are possible are as follows:

Pair of lines 1	Pair of lines 2	
1	∝ Ω	∝ Ω
2	440 Ω	100 Ω
3	400 Ω	50 Ω
4	360 Ω	
5	100 Ω	
6	55 Ω	
7	50 Ω	
8	45 Ω	
9	5.6 Ω	

The network resistances always consist of 2 x R/2 to permit connection of the S_0 feed in the center of the termination value.

TE load

Isolated unity-gain amplifier

Two amplifiers are switched on during the impedance measurement and form the return branch of the AGC in order to hold the S_0 bus transmitted level stable. They are supplied via the internal S_0 feed.

S_0 bus voltage detector

Before each measurement with the internal S_0 feed, the voltage on the S_0 bus is measured with an optocoupler. When the S_0 voltage is found to be $U_{S0} > 16$ V, the internal S_0 feed is not enabled in order to protect the module for possible destruction.

Reference

The measuring panel contains two references for the impedance measurement and for the balance measurement. The reference is first measured before each measurement. The measured values are calculated relative to the reference values. The reference is switched on via relay K7.

2.3 CPU

The main computer is equipped with an Intel microcomputer of type 80C186. This 16-bit system has a 768-kB program memory and a 256-kB data memory. An integral crystal oscillator with 11.0592 MHz acts as the clock generator. An NiCd accumulator feeds the data memory and the clock device when the main power supply is switched off.

Two interrupt controllers (82C59A-2) manage the interrupt signals of the modules. The Intel graphics processor 82786 and a video RAM with 512 kB are integrated on the board for control of the display.

The main functions of the CPU are:

a) User guidance through the individual measuring modes

b) Control of measuring modules

c) Display of measured values

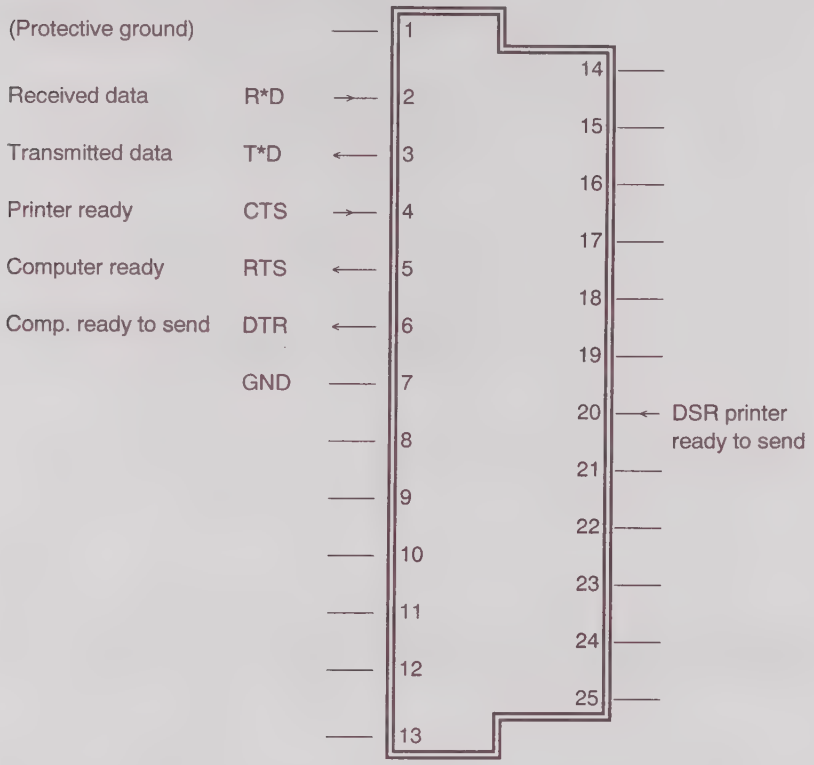
d) Management and storage of measured values

e) Operating the IEC interface

A real-time multitasking operating system ensures problem-free execution of these functions.

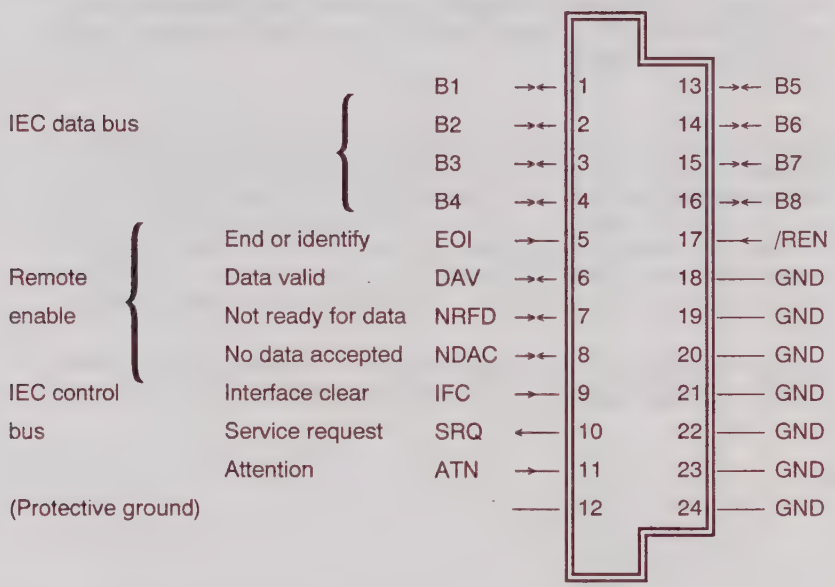
For hardcopies, an external V24 interface (BU 101) is provided for the data transfer between K1403 and the printer or PC. For further information, see section 6.3, "Use of the V.24 interface as printer interface".

Pin assignments of 1st (V24) **serial interface (X95)**



The integrated IEC interface (BU102) can be operated as TALKER and LISTENER according to IEEE 488.2. Via this second interface, it is possible to control the K1403 as well as receive measuring data from the K1403.

Pin assignments of IEC interface (X94)


IEC data bus
B1 1 13 B5
B2 2 14 B6
B3 3 15 B7
B4 4 16 B8
Remote enable
End or identify EOI 5 17 /REN
Data valid DAV 6 18 GND
Not ready for data NRFD 7 19 GND
No data accepted NDAC 8 20 GND
IEC control bus
Interface clear IFC 9 21 GND
Service request SRQ 10 22 GND
Attention ATN 11 23 GND
(Protective ground) 12 24 GND

2.4 Control unit and power supply unit

The control panel is a touch-sensitive display and therefore allows high operating flexibility. It is possible, for example, to arrange the control elements next to or in a graphic results display.

The IR barrier principle was selected from the wide range of design possibilities since, unlike capacitive or resistive systems, it requires no sensitive supplementary glass panes.

Only a matrix of infrared beams (16 x 32) integrated into the display frame is laid over the active display area. If a beam is broken during interrogation, the controller reports this to the main computer, thus initiating verification and security routines.

The lines and columns of the IR matrix are cyclically interrogated for interruption. If an interruption is recognized, the line and column coordinate is moved to a FIFO memory of length '3' which is set up in an internal RAM. A new position is reported only if all three memory positions contain the same line or column coordinates. Thus the output of a new position follows a finger movement. If the IR matrix is exited, a validating message is also output after three interruption-free interrogation cycles.

Besides the infrared matrix, there are six hardkeys which are interrogated individually via port pins in order to ensure unambiguous assingments of inputs in the case of multiple activation. The software recognizes the key last pressed as the most significant one and indicates this after releasing the key. Together with the key T1 (menu), double keys can be formed.

A CPU of the 8031 family is implemented as controller. The chosen type 8751 features an On-Chip-Eprom with a 4 kB program memory. The program only uses the internal RAM with 128 bytes.

Depending on the system, the operating functions may be interfered with if there is a high level of infrared radiation directly onto the display frame (e.g. direct sun- or spotlight).

A primary-clocked power supply unit is used. When supplied, it is set to the line voltage indicated on the rating plate at the rear of the unit. Before switching on, ensure that the operating voltage indicated on the rating plate agrees with the local AC supply. It is possible to switch the unit over to a supply voltage of 230 V or 115 V. This must be done **before using the unit** by means of a screwdriver or coin on the rear panel. In the case of older units which do not have this selector, switching over of the power supply within the unit must only be performed by service personnel.

The AC supply is connected via an inlet connector for non-heating appliances at the rear of the unit. Various regulated DC voltages are available at the secondary output.

–	Output	1	+5.1 V /	12 A
–	"	2	+12 V /	5 A
–	"	3	-12 V /	2 A
–	"	4	-5 V /	1 A
–	"	5	+12 V /	2 A

The fuses (3.15 A slow-blow, 250 V) are located in the housing of the inlet connector for non-heating appliances and can be exchanged without opening the unit.

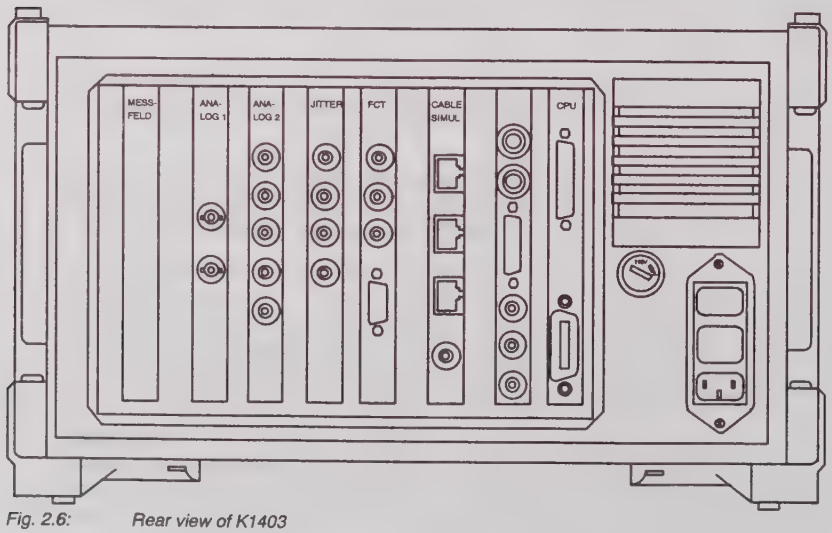


Fig. 2.6: Rear view of K1403

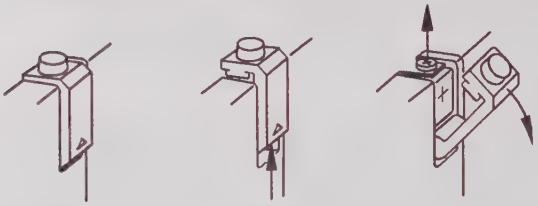
3 Start-up preparations

The following pages will tell you how to make the ISDN S_0 Analyzer ready for use. It will also tell you what you must observe when mounting the K1403 modules.

3.1 Mounting a module

First, remove the cover of the device. The fixing screws for the cover are covered by four corner latches. Proceed as follows:

➤ Push the corner latches some 4 mm upwards in direction of the arrow until you meet resistance and unhinge the corner latches.



➤ Loosen the four screws which are now accessible and remove the cover.

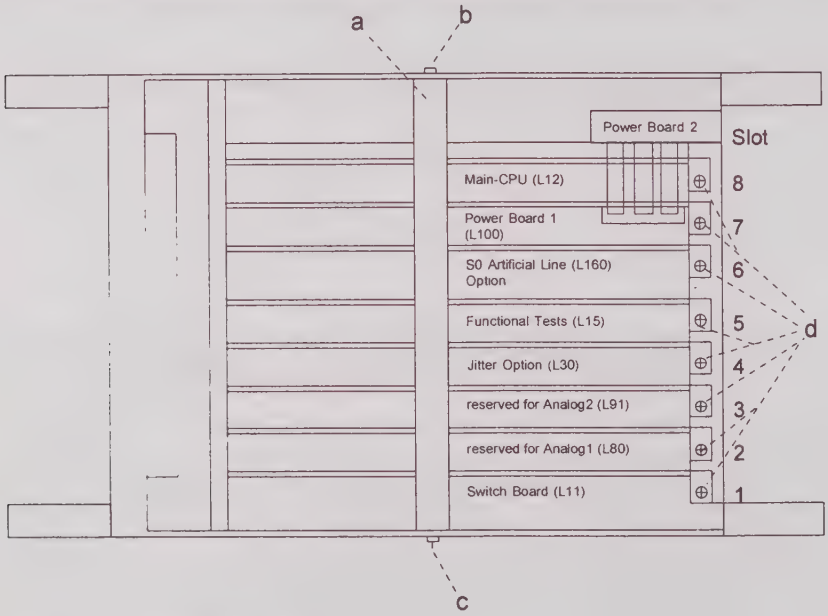


Fig. 3.1: Set-up of the modules

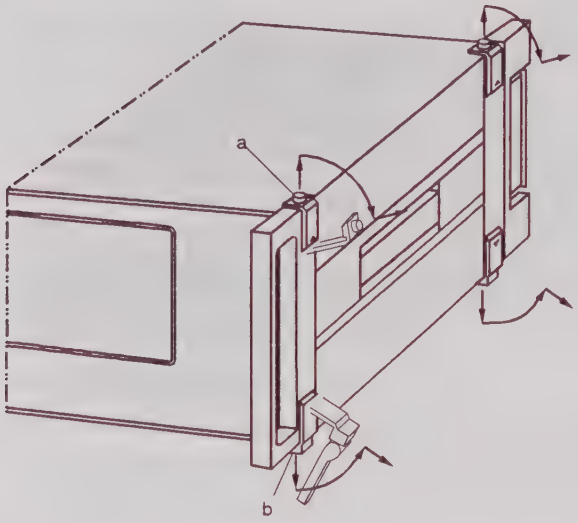
➤ Take the support (a) out by removing screws (b) and (c).

➤ Loosen the module slot screw (d). Insert the module into its destined slot. Ensure that it is correctly assigned and properly fitted in the guide support.

➤ Tighten the module slot screw (d). Re-mount the support (a): Position the printed board in the grooves of the support and tighten screws (b) and (c).

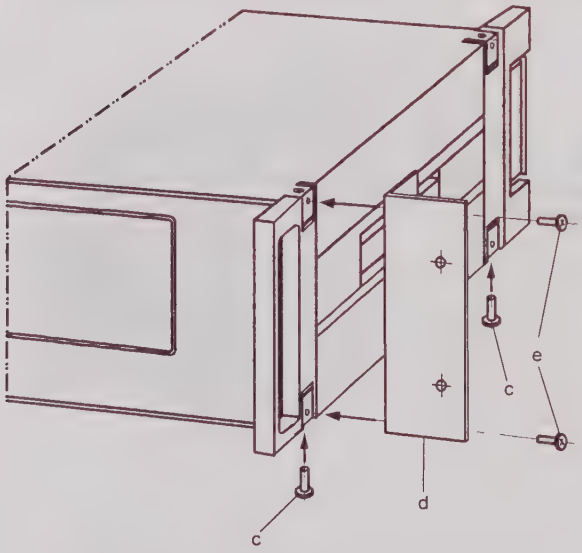
➤ Re-attach the cover of the device.

3.2 Positioning in the 19" rack



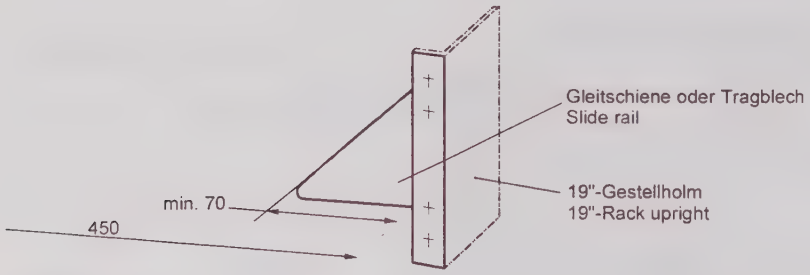
➤ Remove the corner latches (a) by pushing them approx. 4 mm upwards until you meet resistance. Then fold them down and pull them off.

➤ Remove the feet (b) by releasing the screws and pushing the feet approx. 4 mm downwards until you meet resistance. Then fold them down and pull them off.



➤ Secure the bottom of the device using the screws provided (c).

➤ Screw the rack bracket (d) tight using the countersunk screws (e).



➤ Insert a glide rail or support of your choice into the 19" rack and secure the rack bracket onto the 19" rack brace.

3.3 Switching on the device

The unit is set when supplied to the line voltage indicated on the rating plate at the rear of the unit. Before switching on, ensure that the operating voltage indicated on the rating plate agrees with the local AC supply.

The power cable supplied is connected to the inlet connector for non-heating appliances at the rear of the unit. The power plug must be fitted into a power outlet with protective ground contact. The protective effect must not be cancelled by using an extension cable without a protective ground conductor. The ambient temperature must lie between + 5 °C and + 40 °C at the operating location.

Insert the power plug. After switching on the unit using the MAINS switch (S1) on the front of the K1403 housing, the unit boots up. Before the first menu appears, a protocol similar to the following is displayed:

V24A TTLE TTLA IECN FIFO FIF1 FIF2 V240

V1.0 RMX K1403 (C) by SIEMENS AUT E3 1989 Link: 27.08.92 15:29:09

V1.0 RMX Driver (C) by SIEMENS AUT E3 1989 Link: 27.08.92 15:28:32

V3.XX K1403 User (C) by SIEMENS AG -- 1995 -- 1990 Link: dd:mm:yy: hh:mm:ss

This protocol indicates which driver (line 1) has been installed and which boot programs have been executed (lines 2 - 4). If an error is detected during installation, the program comes to a halt and places a "?" at the start and end of the message, e.g. ?V24A?.

Warning!

When using measuring mode "Earth unbalance" (longitudinal balance, LCL), isolation of the electrical ground and protective earth is cancelled for test purposes. The maximum permissible isolation voltage between test sockets BU6 and protective earth and between BU7 and protective earth is 100 V.

Self test

A short equipment self test is performed before moving to the basic menu. This test involves the interrogation of the SW version numbers of the module computers. This prevents communication errors, particularly where optional modules are concerned. The module computers normally log in with the following, e.g. with full unit configuration:

SELF TEST .....

ANALOG1 : SW: V2.00 HW: 1.2 C73249-A11-L8

ANALOG2 : SW: V2.10 HW: 1.0 C73249-A11-L91

FEEDING : SW: V2.01 HW: 1.0 C73249-A11-L100

MEAS.PANEL: O5

FUNCT(1) : SW: V1.00 HW: 1.0 C73249-A11-L15

FUNCT(2) : SW: V2.51 HW: 1.1 C73249-A11-L15

JIT(1) : SW: F2.10 R2.10 HW: 1.0 C73249-A11-L30

CABLE-SIM-L16 HC : 00

In the event of an error, the program reports a '?' (Example: ANALOG1 : ?).

4 Operation

The required measuring mode, the test parameters and all equipment parameters are clearly arranged on a large, self-luminous electroluminescent display and set with the aid of operator prompting (menu technique).

Operator prompting is performed with selection windows and interactively changing softkey combinations. Functions or parameters are selected by simply touching the relevant part of the touch screen. No pressure needs to be exerted. Each selection is acknowledged by inversion and is implemented when the panel is exited.

If several setting parameters are offered, these are combined into a single selection window. This window appears after the parameter, e.g. transmitted level has been selected and is deleted after a value has been selected.

There are only two menu levels: the basic menu (which appears after switch-on) and the working menu. The latter is actively adapted, i.e. expanded or simplified, to the given setting or operating mode (START, STOP, RESULT).

Only those touch panels which are necessary or expedient for an application are faded in. Other possibilities need not be taken into account.

4.1 Control elements and sockets

In addition to the touch screen, the K1403 has only a limited number of other control elements.

Keys

MAINS S1

Mains switch. With the mains switch the analyzer is switched on or off.

MENU T1

With the MENU key, the main menu can always be reached.

RESULT T2

The RESULT key can be used, after a measurement has been made, to display results for further evaluation. Where results are to be displayed in graphic form, for example, a CURSOR-controlled numerical display is called up.

START/STOP T3

The START/STOP key is used for starting/stopping a measurement.

HARDCOPY T4

The HARDCOPY key is used to print a copy of the screen contents on an external printer.

MEMO T5

The MEMO key is used to branch to a menu for selecting measured-value and parameter memories (MEMORY).

PADS LOCK T6

This key locks the touch screen to prevent unintentional actuation, e.g. during continuous measurements. Operation is enabled again when the key is depressed a second time. A status indication (**LOCKED**) appears in the display. The key is enabled only in the measuring mode menus.

Sockets

Protective ground connection BU1

Socket BU1 can be used to connect the protective ground of the K1403 to the reference surface of the test set-up when measuring longitudinal unbalance.

B-IN BU2

B-IN is a contra-directional data input for the B-channels. This socket is assigned to the FUNCTIONAL TESTS module.

(TTL; R_e = 1 kΩ; overvoltage protection against V_{cc} and GND)

B-OUT BU3

B-OUT is a contra-directional data output for the B-channels. This socket is assigned to the FUNCTIONAL TESTS module.

(TTL; R_a = 50 Ω; short-circuit-proof)

CLK BU4

The reference clock is available at output CLK (TTL). The reference clock can be either 64 kbit/s, 128 kbit/s or 144 kbit/s when accessing the B-channels. This socket is assigned to the FUNCTIONAL TESTS module.

(TTL; R_a = 50 Ω; short-circuit-proof)

FSC BU5

Output signal FSC (frame signal clock) is a frame clock for the S0 transmission frame. FSC (TTL) can be used for synchronization tasks. This socket is assigned to the FUNCTIONAL TESTS module.

(TTL; R_a = 50 Ω; short-circuit-proof)

S0 (TAE8+4) BU6/(RJ45) BU7

Sockets BU6 and BU7 are used for connecting the test object to the S0 Analyzer K1403. They are connected in parallel internally.

Supply voltage	Signal	Socket TAE8 + 4	Socket RJ45
$+U_F$ #	S_{REC1} (+)	6	3
$+U_F$ #	S_{REC2} (-)	5	6
$-U_F$ #	S_{TRX1} (+)	3	4
$-U_F$ #	S_{TRX2} (-)	4	5

Signal circuit for NT as per FTZ 1TR230, 386TR2 and T1D1

Polarity for normal mode. (+) and (-) are reversed for Restricted mode.

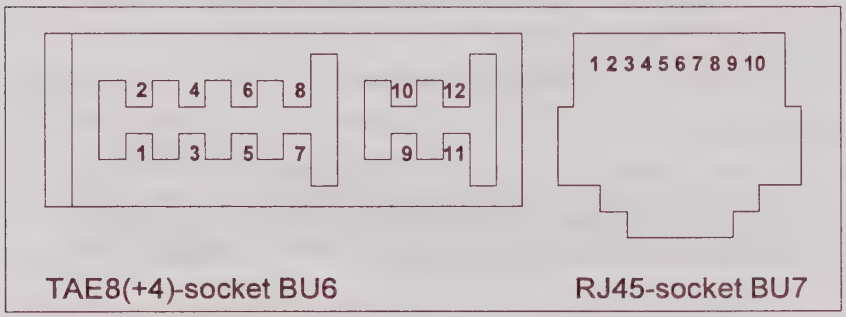


Fig. 4.1: TAE8 and RJ45 socket

The polarity of S0 sockets BU6 and BU7 is reversed internally in accordance with the operating mode (TE, NT).

ANALOG1/ LEVEL METER input BU41

The input signal of the ANALOG1 module is available during the measuring modes Impedance and Unbalance.

Max. input level U_{emax} = 4.4 Vpp (+6 dBm)

Input resistance R_e = 10 kΩ

ANALOG1/ LEVEL METER output BU42

Together with input BU41, transmitter output BU42 is intended for connecting external test set-ups. BU42 supplies a sinusoidal signal which can be set via the menu.

Transmitted signal amplitude U_{rms} = 100 mV ... 1 V

Output resistance Ra ≤ 20 Ω

Where impedance measurements are performed via the measuring panel, the transmitted level varies as a function of the test object and the transmitted frequency since an AGC controller is connected.

ANALOG2 DATA output

The amplified signal of the receive line of the K1403 is available at this socket. This output is provided e.g. for monitoring purposes and subsequent applications.

Output resistance R_i = 75 Ω

Bandwidth BW ≈ 30 MHz

Tolerance Δv = ±0.25 dB to 10 kHz

Measuring mode	Gain
Pulse shape; 5.6 Ω	21.46 dB
Pulse shape; 50 Ω	9.87 dB
Pulse shape; 400 Ω	1.87 dB
Peak current	31.46 dB

Input signal amplification for various measuring modes (ANALOG2)

ANALOG2 M-CLK input

The clock output of the jitter option, an external jitter generator or the output of a through-modulator is connected to this socket. The test pattern generator (INFO generation) can thus be supplied with a jittered system clock in order to jitter the transmitted signal. Switchover to external clock generation is performed in the menu.

Input center frequency f_{center} = 12.288 MHz

Input level Ue: CMOS (no overvoltage protection; R_e = 200 Ω)

ANALOG2 M-CLK output

The clock input of the jitter option or the input of a through-modulator is connected to this socket. The system clock of the ANALOG2 module can then be used as the reference clock for the jitter generator of the jitter option or for a through-modulator.

Output frequency f_{center} = 12.288 MHz

Output level Ua: CMOS (no short-circuit protection; R_i=10 Ω)

ANALOG2 transmitter clock / CLOCK input

This socket is reserved for subsequent applications.

ANALOG2 transmitter clock / CLOCK output

The output supplies the system clock of the test pattern generator (INFO generation). The signal can be passed on to an external through-modulator for jittering.

Output frequency	f_{sys} = 1.54 MHz
Output level	Ua : CMOS (no short-circuit protection!)

This output is reserved for subsequent applications.

The DATA, M-CLK input and M-CLK output sockets must be connected to the corresponding DATA-IN, CLK output and CLK input sockets of the jitter option 7KK1403-2AD if this module is inserted.

Socket IM

Socket IM can be used to measure the load current on the terminal equipment. The output level is:

Ua	= I*{1 Ω, 15 Ω,1 kΩ}	depending on the measuring range set
R_I	≥ 750 kΩ	recommended internal impedance for voltmeter

Sockets U1 (+) / U2 (-)

4.5-mm sockets U1 (+) / U2 (-) can be used to connect an external DC voltage source for feeding the terminal equipment. It is necessary to switch to external feeding in the menu.

Max. input level	U_{emax} = 60 VDC
Max. current	I_{emax} = 200 mA

(+) = red

(-) = black

There is no overload protection for either the test object or the source when external feeding is used. Through-connection is made directly to the test object by means of a relay.

Socket TRG

A trigger signal (TTL level; 50 Ω; short-circuit-proof) is output at socket TRG to trigger an external oscilloscope or transient recorder.

The symbol on the module label has been printed incorrectly on certain modules. An input symbol has been used instead of an output symbol

Socket ANL

An external signal which can be measured using the built-in transient recorder can be connected to the socket ANL (analog in).

Input voltage range 0..300 mV; R_e > 500 kΩ; U_{emax} = ± 5 V.

Socket X6

This socket routes signals for controlling external components in the test set-up or enables further external connections for the K1403 test set.

Pin no.	Name	Type	Assignment
1	GND-D	---	Digital ground
2	I0	Output	User interface CMOS level; no short-circuit fuse
3	I1	Output	
4	I2	Output	
5	I3	Output	
6	I4	Output not used	
7	I5	Output	
8	free	---	
9		not used	
10		not used	
11		not used	
12		not used	
13	GND-A	---	Analog ground
14	TRIG	Input not used	TTL level; for triggering the internal transient recorder
15	+5 V	Output	Power supply for external HW; no fuse

V.24 BU101

The V.24 interface is set to the following values:

Baud rate : 9600

Data bits : 8

Stop bits : 1

Parity : No parity check

Pin no.	Name	Type	Assignment
1	SL	---	Protective ground
2	RxD_N	Input	Received data
3	TxD_N	Output	Transmitted data
4	CTS	Input	Printer ready
5	RTS	Output	Computer ready
6	DTR	Output	Computer ready to send
7	GND	---	Ground
20	DSR	Input	Printer ready to send

IEC 625 BU102

Refer to Section 5 for a detailed description of the IEC interface.

Pin no.	Name	Type	Assignment
1-4 13-16	B1_N - B8_N	Bi-directional	IEC data bus
5	EOI_N	Input	End of identify
6	DAV_N	Bi-directional	Data valid
7	NRFD_N	Bi-directional	Not ready for data
8	NDAC_N	Bi-directional	No data accepted
9	IFC_N	Input	Interface clear
10	SRQ_N	Output	Service request
11	ATN_N	Input	Attention
12	SL	---	Protective ground
17	REN_N	Input	Remote enable
18-24	GND	---	Ground

4.2 Summary of operation

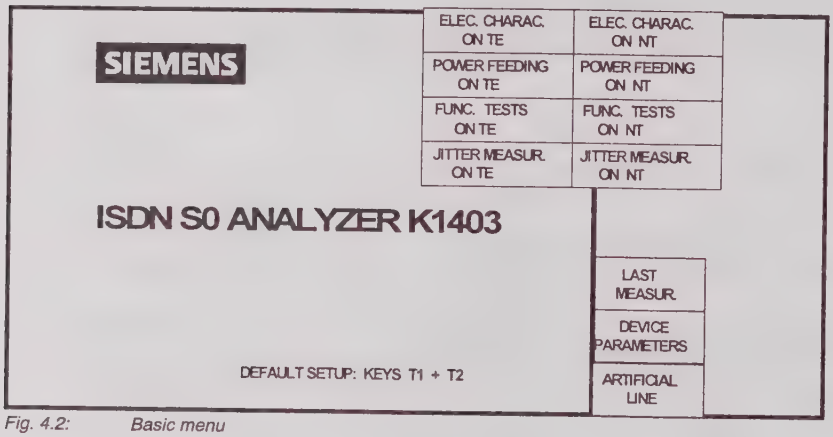


Fig. 4.2: Basic menu

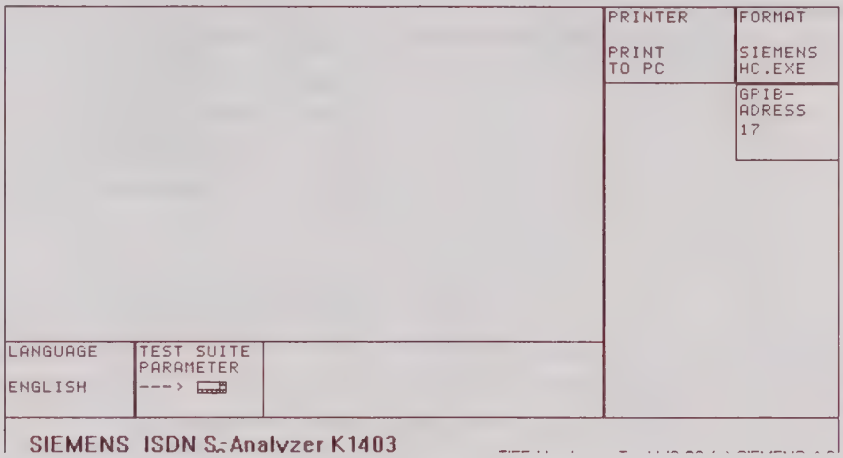
The self test is carried out when the analyzer is switched on. The basic menu is displayed when the self test has been completed successfully. In the basic menu you can

1) select between measurements on the TE or NT,
2) recall the last measuring mode that was terminated using STOP,
3) change to the device parameter menu,
4) set the artificial line option - if inserted - on its own without the selected measuring mode (see manual for artificial line 7KK1403-2AA).

It is always possible to return to this basic menu by pressing the MENU key once or several times

The analyzer can be initialized by simultaneously pressing keys MENU and RESULT in this screen. This is necessary following a repair or conversion.

4.2.1 Device parameters



Setting parameters (MENU)

BASIC MENU	LANGUAGE	TEST SUITE PARAMETER	PRINTER	FORMAT	IEC BUS ADDRESS
LAST MEASUREMENT	GERMAN	MENU DISPLAY	IBM	NORMAL	EDIT
DEVICE PARAMETERS	ENGLISH		EPSON (STANDARD)	TURNED BY 90°	
ARTIFICIAL LINE			PRINT TO PC		

Generally, printers of IBM or EPSON graphics format are used. Selecting "Printout to PC" causes the transmission of data in a special format to the PC.

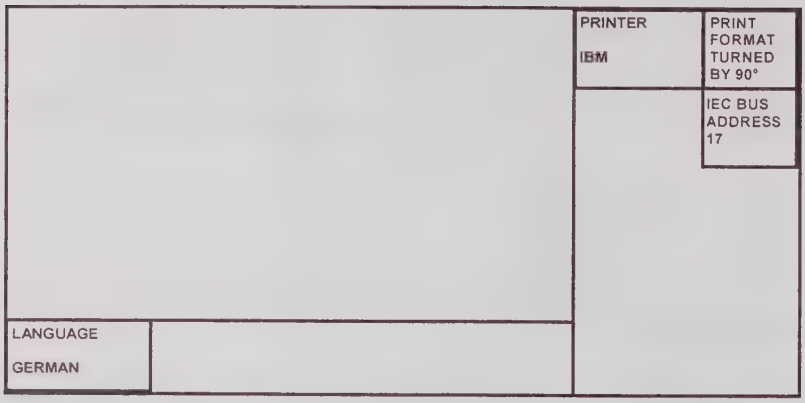
For a hardcopy of the display, a printer or a PC must be connected to the V.24 interface of the device. The circuits of this interface are selected such that the device can operate as a peripheral unit (single-ended) for a controller (PC). In the case of a direct connection of a printer or a PC with a V.24 interface, this means that the pin assignment of the transmission lines may have to be changed (see section 9.4 "Use of the V.24 interface as printer interface").

Please note the current information in the **readme.txt** file on diskette.

The TEST SUITE PARAMETER are described in the user manual **Functional Tests**.

Extension of device parameters as of software version V3.01

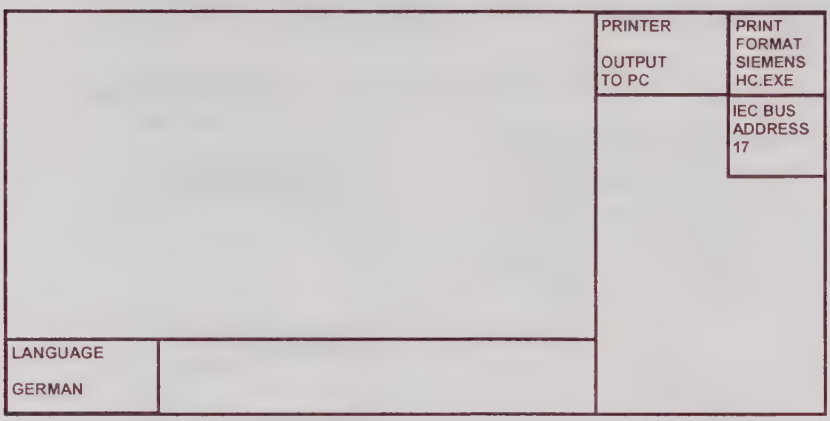
Output to printer



Setting parameters (MENU)

BASIC MENU	LANGUAGE	PRINTER	PRINT FORMAT	IEC BUS ADDRESS
LAST MEASUREMENT	GERMAN	IBM	NORMAL	EDIT
DEVICE PARAMETERS	ENGLISH	EPSON (STANDARD)	TURNED BY 90°	
ARTIFICIAL LINE		OUTPUT TO PC		

Output to PC



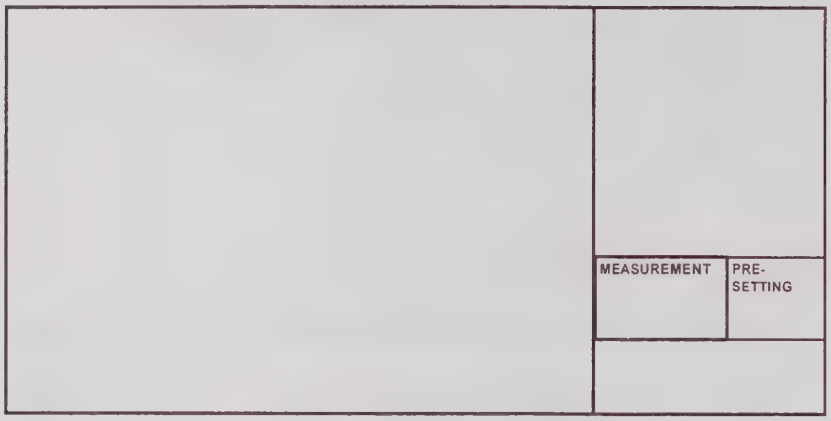
Setting parameters (MENU)

BASIC MENU	LANGUAGE	PRINTER	PRINT FORMAT	IEC BUS ADDRESS
LAST MEASUREMENT	GERMAN	IBM	SIEMENS HC.EXE	EDIT
DEVICE PARAMETERS	ENGLISH	EPSON (STANDARD)	TIFF	
ARTIFICIAL LINE		OUTPUT TO PC		

Please note the current information in the **readme.txt** file on diskette.

4.3 Loading and saving the measurements

After pressing the MEMO key, the menu for storing measured values and parameters appears.

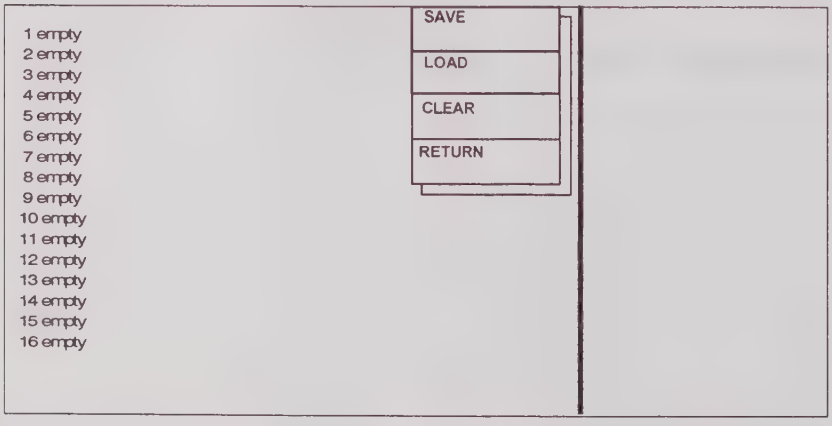


MEASUREMENT

16 different measurement curves or numerical values can be stored with (SAVE) and reloaded into the display as required with (LOAD).

PRESETTING

16 different complete device settings can be stored. Each user can file device settings in memories 1 to 16 for repeated measurement tasks. The preset contents then only need to be loaded by selecting the corresponding memory.



Use SAVE to store the test results.

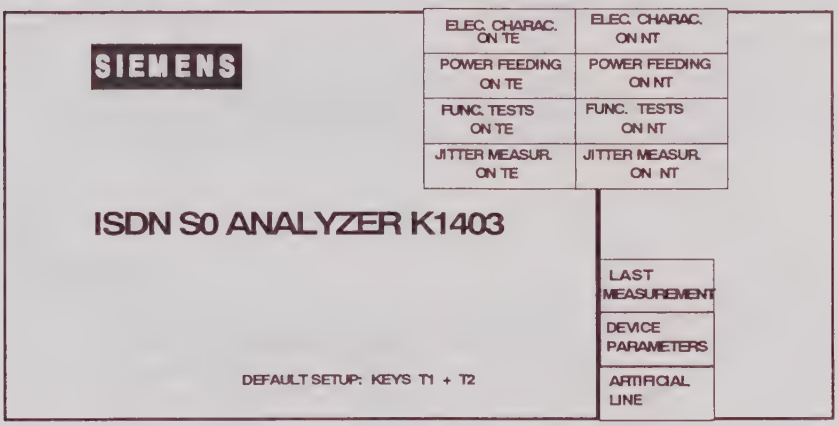
Use LOAD to load the stored values into the display.

Use CLEAR to delete the memories either singularly or altogether.

Use RETURN to return to the last test menu that was called up.

Basic initialization of the equipment is performed if keys T1 + T2 are pressed simultaneously while the basic menu is displayed. In the unit, the setting parameters are then set to the relevant default values.

Load last test result



After selecting the `Last measurement` field, the last test result can be loaded and is displayed on the screen.

5 Measurements and presentation of results

5.1 Power feeding conditions TE

The following applies to all measurements of power feeding conditions: an offset adjustment of the current and voltage measuring ranges is carried out automatically every 30 minutes, but not during a running measurement.

Warning!

Please note that the device may be destroyed if an external voltage source is connected for any measuring mode, especially the measuring mode power consumption on TE with the supply PS2, since no interference voltage check is carried out before starting this measurement.

5.1.1 Power consumption

(ETS §D.5.1.1.X, D.5.1.2.X)

				SERIAL RESISTOR 0.0Ω	S0-R 50Ω
				RANGE SELECT 0...230mA	
				MEAS: AFTER PWR. UP 3.0 s	
MEASUREM. (TE) POWER CONSUMPTION	STATE NOT ACTIVATED	POWER FEEDING NORMAL PS1		VOLTAGE 24.0 V	

Setting parameters (MENU)

MEASURE-MENT	STATE	POWER FEEDING	STATUS Fx	SERIAL RESISTOR	RANGE SELECT	MEAS. AFTER PWR-UP.
POWER CON-SUMPTION	NOT ACTIVA-TED	NORMAL PS1	F2	EDIT	0...230 mA	EDIT
CURRENT/ TRANSIENT MEASUREMENT	MEAS. → Fx	RESTRIC-TED PS1	F3	LAST EDIT VALUE	0...38 mA	LAST EDIT VALUE
CURRENT/TIME MEASUREMENT	MEAS Fx →	NORMAL PS2	F4	0 Ω	0...6 mA	3 s
POWER START-UP TESTS		RESTRIC-TED PS2	F5		0...750 µA	
SWITCHOVER TESTS			F6		0... 90 µA	
SHORT INTERRUPTION			F7			
			F8			
			UPSTREAM			
			DOWN-STREAM			

VOLTAGE	S0 - R
EDIT 10 ... 56.5 V	50Ω
LAST EDIT VALUE	100Ω
24 V	
32 V	
42 V	

Warning!

During the measurement power consumption the electrical isolation between the measuring unit power feeding conditions (L100) and the internal ground potential is cancelled. In the case of a faulty measurement setup, a short circuit may occur. When using a non-isolated IEC bus card the electrical isolation between internal ground and protective ground is also cancelled.

Dependencies of key "Status Fx":

NOT ACTIVATED	MEAS)1 → Fx	MEAS)2 Fx →	INFORM. TRANS. CAPABILITY	CHANNEL	P.NUMBER > SUB.ADR. >
---	F2..F8	F2..F8			
---	UPSTREAM	UPSTREAM	SPEECH	B1	P.NUMBER
---	DOWN-STREAM	DOWN-STREAM	AUDIO 3.1KHZ	B2	SUB.ADR.
			DATA		CLEAR
			AUDIO 7KHZ		RETURN
			VIDEO		

)1 Measurement before change in status
)2 Measurement following achievement of status Fx

You can either select the offered states (F-states) of layer 1 or the complete activation of layer 1, 2 and 3:

⇒ Fx
⇒ UPSTREAM
⇒ DOWNSTREAM

In case of UPSTREAM, the K1403 waits for a basic interconnection test initiated by the TE, in case of DOWNSTREAM, the K1403 runs this test on its own.

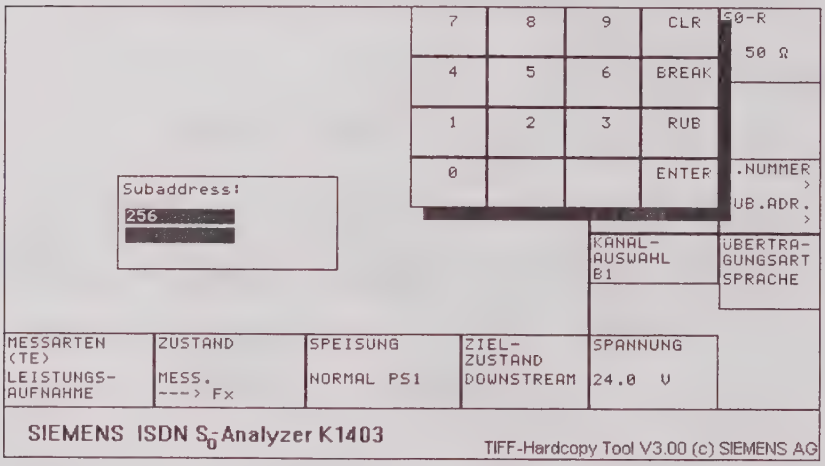
CHANNEL

With this parameter you select the B-channel to be determined (B1 or B2). This channel is connected to the BU2-BU5 sockets and thus it is available for the connection to an external data source/sink.

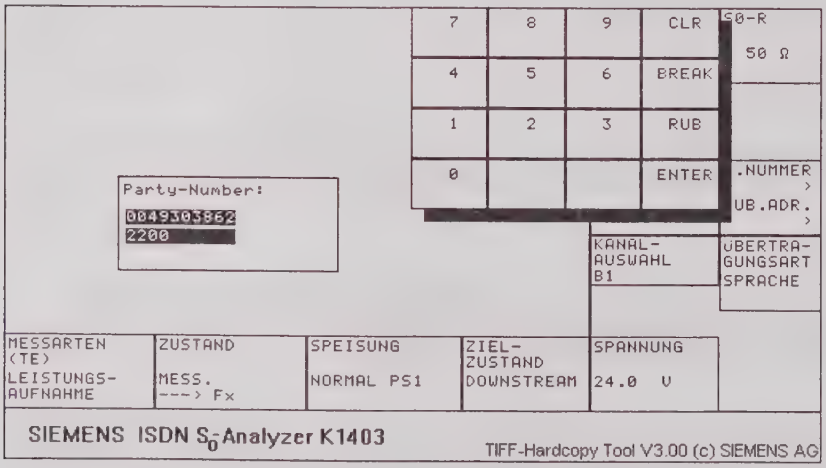
To the B-IN, B-OUT, CLK and FSC sockets e.g. a semi-channel test set such as the SIEMENS P2112 can be connected. With this it is possible e.g. to connect test tones to the telephone set and thus you can test the influence on the maximum power input or on current transients.

P.Number / Sub.Adr.

With this key your are given the possibility for an input of a 20-digit call number (Called Party Number) and a 20-digit extension number (Called Party Subaddress). The input is carried out via an editing window. Afterwards you leave the input window with the RETURN key.



After touching the P. NUMMER field you get the editing field for a 20-digit call number. Enter the desired value and terminate this procedure with ENTER.



If you have pressed the SUB.ADR. key, you can enter a 20-digit number with which a specific terminal at a private branch network can be selected.

`Information transmission capability`

An element of the SETUP message, with which the basic interconnection test of layer 3 is initiated, is the information transmission capability (Bearer Capability). With this parameter the service is determined on which the connection shall be based. The following selection can be made.

- Speech
- AUDIO 3.1kHz
- Data
- AUDIO 7.0kHz

Video

Measured quantity

The parameter is the supply current of the TE. The test object is either in the activated or deactivated state (selectable in menu).

Test method

The test object is supplied with an adjustable DC voltage PS1. The current is measured in the circuit. Following output of the DC voltage, the least sensitive measuring range is initially set for an adjustable delay time T1.

Measurement without activation:

T0: Time of voltage output
T1: Start of measurement
D : Delay time (0 to 12 s); measurement following switching on

The selected current measuring range is activated following this time, and the delay time T2 allowed to expire.

Measurement prior to achievement of selected TE state Fx:

T0: Time of voltage output
T1: Start of measurement
T2: Start of TE state change
D1: Delay time (adjustable from 0 to 12 s); measurement following switching on
D2: Delay time approx. 6 s

Measurement following achievement of selected TE state Fx:

T0: Time of voltage output and activation of TE
T1: TE is in state Fx
T2: Start of measurement
D: Delay time (adjustable from 0 to 12 s); measurement following achievement of selected TE state Fx

The current is measured every 2 ms following expiry of time T1 + T2. These measured values are used for the "quasi" real-time power calculation. The current values measured over a period of 50 ms are averaged for the MIN/MAX power and current consumptions. Averaging is carried out over a period of 500 ms to produce the average power and current consumptions.

The minimum/maximum current and power values are calculated again following activation of the softkey: MIN/MAX values NEW. It is possible to enter the line resistance (if present) for the connection cable from the TE to the Analyzer. This value is then taken into consideration during the power calculation.

Measurement (START/STOP)

The START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module L100 are initialized. The following status message appears in the display

`INIT/START`

The start of the measurement is indicated by

`MEASURE`

Then....

- the K1403 asks the user to initiate a connection (<USER CALL>), if the parameter STATE was set to UPSTREAM,
- or it is necessary to accept the call, i.e. to acknowledge the connection if the parameter STATUS was set to DOWNSTREAM.

As soon as the basic interconnection test is terminated, this is signalled with the message <FKT: connect downstream> or with the message <FKT: connect upstream>.

In accordance with ETS 300_012 it is required that during the feeding tests local actions are carried out at the test object. It is also recommended to select those which lead to especially high power consumptions or power changes (e.g. switch-on of loadspeakers, set bell to max. volume etc.).

The START/STOP key must be depressed again to stop the measurement. The following appears

STOP

Presentation of results (RESULT)

During the measurement, the result appears in the form

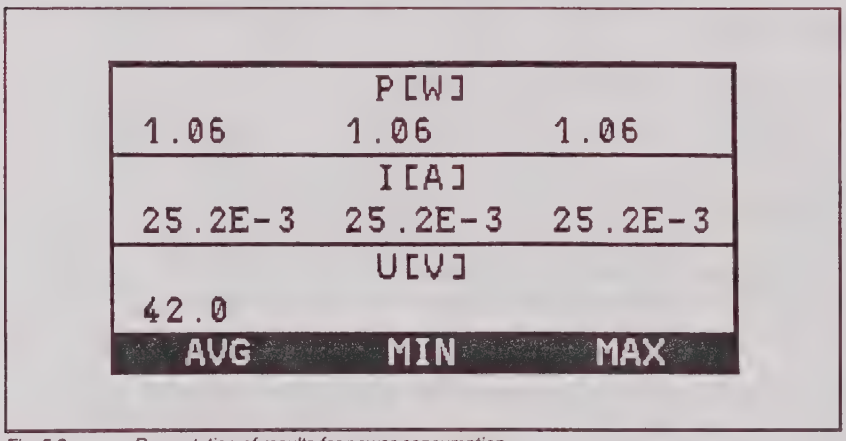


Fig. 5.3: Presentation of results for power consumption

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.1.2 Current/transient measurement

(ETS §D.5.1.3)

				RANGE SELECT 0..70mA	SIGNAL SOURCE INTERNAL
				SAMPLING RATE 10MHz T = 25,0 µs	TRIGGER-GRADIENT 5mA/µs
				TRIGGER SLOPE POSITIVE	
MEASUREMENT (TE) CUR. / TRANS. MEASUREMENT	POWER FEEDING NORMAL		STATUS Fx F3	VOLTAGE 42.0 V	

Setting parameters (MENU)

MEASUREMENT
POWER CONSUMPTION
CURRENT TRANSIENT MEASUREMENT
CURRENT TIME MEASUREMENT
POWER START-UP TESTS
SWITCHOVER TESTS
SHORT INTERRUPTION

POWER FEEDING	STATUS Fx	RANGE SELECT	SIGNAL SOURCE
NORMAL	F3	0 ... 70 mA	INTERNAL
RESTRICTED	F4	0 ... 23 mA	EXTERNAL 0 ... 0.4 V
	F5		
	F6		
	F7		
	F8		
	UP-STREAM		
	DOWN-STREAM		

SAMPLING RATE	TRIGGER-GRADIENT	TRIGGER SLOPE	VOLTAGE	INFORM. TRANS. CAPABILITY	CHANNEL	P.NUMBER > SUB.ADR. >
5 MHZ T = 50.0 µs	3.0 mA/µs	POSITIVE	EDIT	SPEECH	B1	P.NUMBER
10 MHZ T = 25.0 µs	3.5 mA/µs	NEGATIVE	LAST EDIT VALUE	AUDIO 3.1KHZ	B2	SUB.ADR.
	4.0 mA/µs		24 V	DATA		CLEAR
	4.5 mA/µs		32 V	AUDIO 7KHZ		RETURN
	5.0 mA/µs CCITT		42V	VIDEO		
	5.5 mA/µs					
	6.0 mA/µs					
	6.5 mA/µs					
	7.0 mA/µs					

The parameters INFORMATION TRANSMISSION CAPABILITY, CHANNEL and P.NUMBER/ SUB.ADR. are only displayed in the menu if UPSTREAM or DOWNSTREAM were selected for the parameter STATE.

Warning!

During the currrent/transient measurement the electrical isolation between the measuring unit power feeding conditions (L100) and the internal ground potential is cancelled. In the case of a faulty measurement setup, a short circuit may occur. When using a non-isolated IEC bus card the electrical isolation between internal ground and protective ground is also cancelled.

Measured quantity

The measured quantity is the rise in the supply current of the test object with different activation states.

Test method

The rise in current is measured by a trigger circuit which is able to record fast current gradients (the trigger threshold is adjustable) and to apply them as a trigger signal to an 8-bit transient recorder. This transient recorder with a selectable sampling rate is armed at the start of the measurement and starts recording when a trigger event is detected. The analog input signal is digitized by an 8-bit A/D converter, and the digital values written into a 4-KByte RAM. The gradient ($\left|\frac{di}{dT}\right|$, where T=1 μs) of the measured current is calculated via software. The current/time characteristic is displayed graphically, if this gradient is greater than the trigger gradient selected by the user.

Measurement (START/STOP)

The START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module L100 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be depressed again to stop the measurement. The following appears:

```
STOP
```

Presentation of results (RESULT)

During the measurement, the result appears in the form:

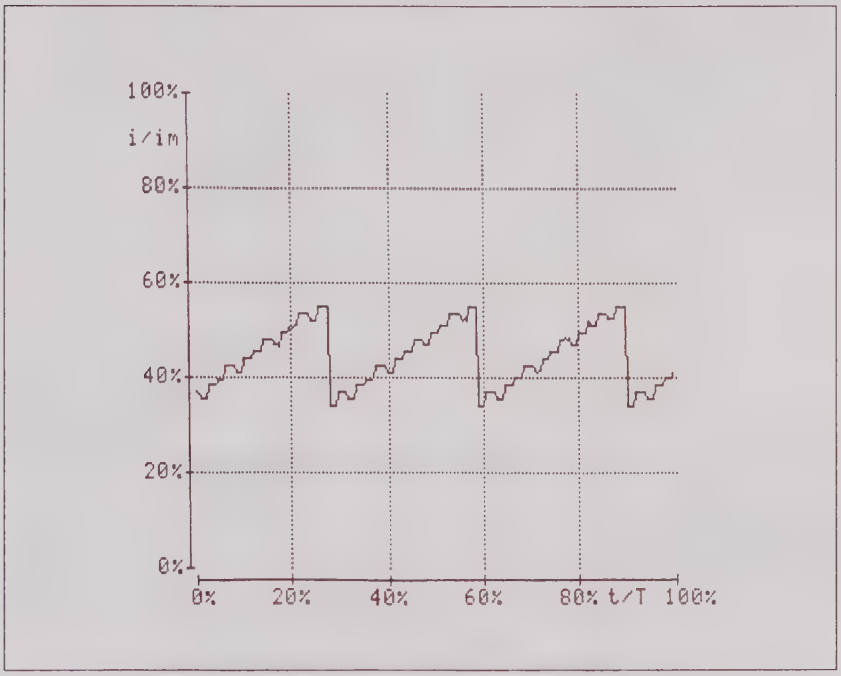


Fig. 5.4: Presentation of results for current/transient measurement

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.1.3 Current/time measurement

(ETS §D.5.1.4.X)

Slow sampling

			RANGE SELECT 0..230mA	
			MEASURING TIME T = 1 s	
			SAMPLING SLOW	
MEASUREMENT (TE) CURRENT / TIME MEASUREMENT	POWER FEEDING NORMAL		VOLTAGE 42.0 V	

Setting parameters (MENU)

MEASURE-MENT	POWER FEEDING	RANGE SELECT	MEASURING TIME	SAMPLING	VOLTAGE
POWER CONSUMPTION	NORMAL	0 ... 230 mA	T = 25 ms	**SLOW**	EDIT
CURRENT/ TRANSIENT MEASUREMENT	RESTRICTED	0 ... 70 mA	T = 125 ms	FAST	LAST EDIT VALUE
CURRENT/ TIME MEASURE-MENT		0 ... 38 mA	T = 250 ms		40 V
POWER START-UP TESTS		0 ... 6 mA	T = 500 ms		
SWITCHOVER TESTS		0 ... 750 µA	T = 1 s		
SHORT INTERRUPTION		0 ... 90 µA	T = 2 s		
			T = 4 s		
			T = 8 s		

Fast sampling

			RANGE SELECT 0..230mA	
			SAMPLING RATE 10MHz T = 25µs	
			SAMPLING FAST	
MEASUREMENT (TE) CURRENT / TIME MEASUREMENT	POWER FEEDING NORMAL		VOLTAGE 42.0 V	

Setting parameters (MENU)

MEASURE-MENT	POWER FEEDING	RANGE SELECT	SAMPLING RATE	SAMPLING	VOLTAGE
POWER CONSUMPTION	NORMAL	0 ... 250 mA	10 MHz T = 25.0 µs	SLOW	EDIT
CURRENT/ TRANSIENT MEASUREMENT	RESTRICTED	0 ... 70 mA	5 MHz T = 50.0 µs	**FAST**	LAST EDIT VALUE
CURRENT/ TIME MEAS.		0 ... 23 mA	2 MHz T = 125.0 µs		40 V
POWER START-UP TESTS		0 ... 5.5 mA	1 MHz T = 250.0 µs		
SWITCHOVER TESTS		0 ... 350 µA	0.5 MHz T = 500.0 µs		
SHORT INTERRUPTION		0 ... 5.5 mA at 70 Ω			

Warning!

During the currrent/time measurement the electrical isolation between the measuring unit power feeding conditions (L100) and the internal ground potential is cancelled. In the case of a faulty measurement setup, a short circuit may occur. When using a non-isolated IEC bus card the electrical isolation between internal ground and protective ground is also cancelled.

Measured quantity

The measured quantity is the supply current to the test object following switching-on of the voltage PS1.

Test method

The measurement starts when the editable voltage PS1 is switched on. This is signalled by a trigger pulse at the rear socket TRIG for controlling an external oscilloscope. The following table shows the relationship between recording duration, number of measured values and sampling time for "slow" sampling.

Recording duration	Number of measured values	Sampling time
8 s	4000	2 ms
4 s	4000	1 ms
2 s	4000	500 µs
1 s	4000	250 µs
500 ms	2000	250 µs
250 ms	1000	250 µs
125 ms	500	250 µs
25 ms	250	100 µs

In the case of fast sampling, 250 measured values are recorded at the rate set by the user.

In each of the measuring ranges selected, the voltage across the corresponding precision resistor can be measured using an external storage oscilloscope (DSO) (at rear socket IM). The DSO is triggered by the trigger signal referred to above.

Measurement (START/STOP)

The START/STOP key is used to start the measurement. Firstly, the measuring panel and the module FEEDING CONDITION (L100) are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

Presentation of results (MENU)

At the end of the measurement, the result appears in the form:

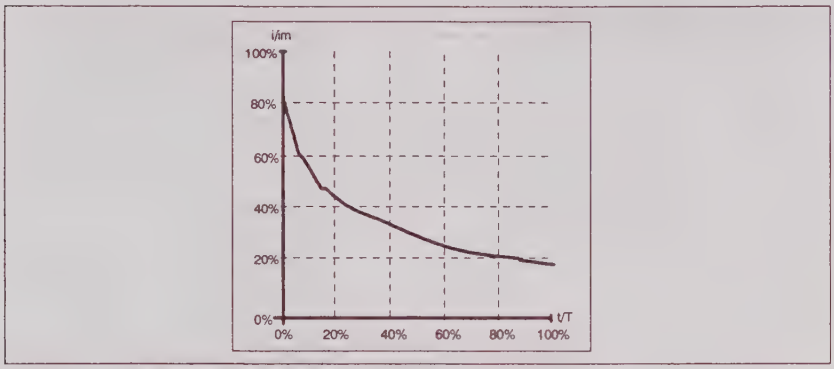


Fig. 5.5: Presentation of results for the current/time measurement

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

During fast sampling oscillations may occur in the measuring range of 0...5.5 mA with capacitive loads C_L > 1 nF.

The following serial precision resistors are switched for slow and fast sampling:

Slow sampling:

Measuring range	Precision resistor
0 .. 230 mA	1 Ω
0 ... 70 mA	15 Ω
0 ... 38 mA	15 Ω
0 ... 6 mA	66 Ω
0 ... 750 µA	1 k
0 ... 90 µA	4 k75

Fast sampling:

Measuring range	Precision resistor
0 .. 250 mA	1 Ω
0 ... 70 mA	15 Ω
0 ... 23 mA	15 Ω
0 ... 5.5 mA	15 Ω
0 ... 350 µA	1 k
0 ... 5.5 mA	70 Ω

5.1.4 Power start-up tests

(ETS §D.5.1.4.4.X)

Following short circuit (ETS network)

				S0-R 50Ω	
				SOURCE TYPE ETS NETWORK	
				TEST MODE TEST A ETS 300012	
MEASUREMENT (TE) POWER START-UP TESTS	POWER START-UP MODE AFTER REM. OF SHORT CIRCUIT	POWER FEEDING NORMAL		U [end] 42.0 V	

Setting parameters (MENU)

MEASUREMENT
POWER CONSUMPTION
CURRENT/ TRANSIENT MEASUREMENT
CURRENT/TIME MEASUREMENT
POWER START-UP TESTS
SWITCHOVER TESTS
SHORT INTERRUPTION

POWER START-UP MODE	POWER FEEDING	S0 - R	SOURCE TYPE	TEST MODE	U [end]
AFTER REM. OF SHORT CIRCUIT	NORMAL	50 Ω	**ETS NETWORK**	TEST A ETS 300012	EDIT
AT LOW INPUT VOLTAGE	RESTRICTED	100 Ω	CURRENT LIMITA-TION	TEST B ETS 300012	LAST EDIT VALUE

After rem. of short circuit (current limitation)

				S0-R 50Ω	
				TYPE OF SOURCE CURRENT LIMITATION	
				CURRENT LIMITATION 9mA	
MEASUREMENT (TE) POWER START-UP TESTS	POWER START-UP MODE AFTER REM. OF SHORT-CIRCUIT	POWER FEEDING NORMAL		U [end] 42.0 V	

Setting parameters (MENU)

MEASUREMENTS	POWER START-UP MODE	POWER FEEDING	S0 - R	SOURCE TYPE	CURRENT LIMITATION	U [end]
POWER CONSUMPTION	**AFTER REM. OF SHORT-CIRCUIT**	NORMAL	50 Ω	ETS NETWORK	EDIT	EDIT
CURRENT TRANSIENT MEASUREMENT	AT LOW INPUT VOLTAGE	RESTRICTED	100 Ω	**CURRENT LIMITATION**	LAST EDIT VALUE	LAST EDIT VALUE
CURRENT TIME MEASUREMENT					9 mA	
POWER START-UP TESTS					11 mA	
SWITCHOVER TESTS					72 mA	
SHORT INTERRUPTION						

At low input voltage

			S0-R 50Ω
MEASUREMENT (TE) POWER START-UP TESTS	POWER START-UP MODE AT LOW INPUT VOLTAGE		VOLTAGE 28.0 V

Setting parameters (MENU)

MEASUREMENT
POWER-CONSUMPTION
CURRENT/ TRANSIENT MEASUREMENT
CURRENT/TIME MEASUREMENT
POWER START-UP TESTS
SWITCHOVER TESTS
SHORT INTERRUPTION

POWER START-UP MODE	S0 - R	VOLTAGE
AFTER REM. OF SHORT CIRCUIT	50 Ω	EDIT
AT LOW INPUT VOLTAGE	100 Ω	LAST EDIT VALUE
		28 V

The circuit according to ETS § D.5.1.4.4.1 is simulated completely in the device.

Dependencies

The following dependencies exist in this menu:

SOURCE TYPE	
ETS NETWORK	CURRENT LIMITATION
ETS 300012 TEST A	EDIT
ETS 300012 TEST B	LAST EDIT VALUE
-	9 mA
-	11 mA
-	72 mA

Measured quantity (ETS §D.5.1.4.4.1.)

Response of a TE test object after rectification of a short circuit.

Test method

a) Method ETS NETWORK

The test object is supplied with a voltage from the PS1 via a test circuit preselected according to ETS 300012. The TE is stimulated via INFO2 during the voltage output. The sequence of the layer 1 protocol is documented on the screen.

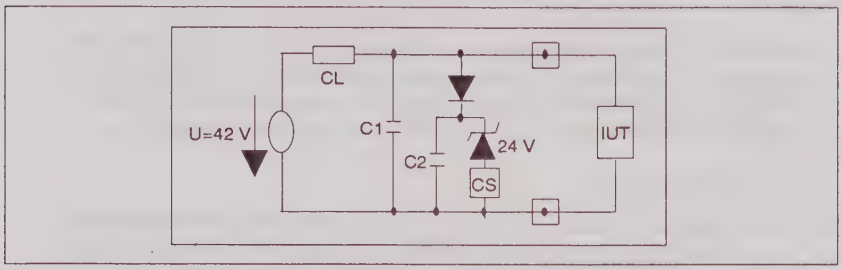


Fig. 5.6: Measuring circuit of power start-up test

Mode of operation / test case

Restricted operation

Test a:	CL = 9 mA ± 0.2 mA	C1 = 0 µF	C2 = 0 µF	CS = 0 mA
Test b:	CL = 11 mA ± 0.2 mA	C1 = 300 µF	C2 = 0 µF	CS = 0 mA

Normal operation

Test a:	CL = 72 mA ± 1 mA	C1 = 0 µF	C2 = 300 µF ± 5 %	CS = 45 mA ± 1 mA
Test b:	CL = 72 mA ± 1 mA	C1 = 300 µF ± 5 %	C2 = 300 µF ± 5 %	CS = 45 mA ± 1 mA

b) Voltage type: current source

To execute the test for restricted operation according to (ETS §D.5.1.4.4.1 Test a) an editable current source is made available. The TE is stimulated via INFO 2 during the voltage output. The sequence of the layer 1 protocol is documented on the screen. P, I, U are indicated approx. every second.

Measured quantity (ETS §D.5.1.4.4.2.)

Response of a TE test object during power start-up with low voltage.

Test method

To execute the test for restricted operation according to (ETS §D.5.1.4.4.2) the test object is supplied with an editable voltage PS1 via a serial resistor (70 Ω). The TE is stimulated via INFO 2 during the voltage output. The sequence of the layer 1 protocol is documented on the screen. P, I, U are indicated approx. every second.

Measurement (START/STOP)

The START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the power feeding module are initialized. The following status message appears in the display

`INIT/START`

The start of the measurement is indicated by

`MEASURE`

Presentation of results

During the measurement the currently measured values P[W] I[A] and U[V] were displayed. At the end of the test, „Test ok" / „Test failed" shows if a layer-1 connection was established (State F7) or not.

Measuring accuracy

See Appendix "Technical data for the power feeding conditions"

5.1.5 Switchover tests

(ETS §D.5.1.4.6)

Normal to restricted operation

(ETS §D.5.1.4.6.1)

				CURRENT LIMITATION 11mA	S0-R 50Ω
				SW. TCN OVER TIME 5ms	P.NUMBER > SUB.ADR. >
				CHANNEL SELECTION B1	INFORM. TRANS. CAPABILITY SPEECH
MEASUREMENT (TE) SWITCHOVER TESTS	MODE NORMAL --> RESTRICTED	CONTROL INTERNAL SWITCHOVER MANUAL	BASIC INTERCONN. TESTS UPSTREAM	VOLTAGE (NORMAL) 32.0 V	VOLTAGE (RESTR.) 40.0V (-)

Setting parameters (MENU)

MEASUREMENT
POWER CONSUMPTION
CURRENT/ TRANSIENT MEASUREMENT
CURRENT/TIME MEASUREMENT
POWER START-UP TESTS
SWITCHOVER TESTS
SHORT INTERRUPTION

MODE	CURRENT LIMITATION	BASIC INTERCONN. TESTS	S0 - R	SWITCHOVER TIME
NORMAL ---> RESTRICTED	EDIT 1 ..30 mA	UPSTREAM	50 Ω	EDIT 5 ... 250 ms
RESTRICTED --->NORMAL	LAST EDIT VALUE	DOWNSTREAM	100 Ω	LAST EDIT VALUE
	11 mA			5 ms

VOLTAGE (NORMAL)	VOLTAGE (RESTRICTED)	CONTROL	INFORMATION TRANSMISSION CAPABILITY	CHANNEL	P.NUMBER > SUB.ADR. >
EDIT	EDIT	EXTERNAL SWITCHOVER MANUAL	SPEECH	B1	P.NUMBER
LAST EDIT VALUE	LAST EDIT VALUE	INTERNAL SWITCHOVER MANUAL	AUDIO 3.1KHZ	B2	SUB.ADR.
24 V	RESTRICTED 32 V	INTERNAL SWITCHOVER AUTOM.	DATA		CLEAR
32 V	RESTRICTED 40V		AUDIO 7KHZ		RETURN
			VIDEO		

The parameters CONTROL, INFORMATION TRANSMISSION CAPABILITY, CHANNEL as well as P.NUMBER /SUB.ADR. are only offered if the switchover MODE was set to NORMAL--> RESTRICTED. See also section 5.1.1.

Measured quantity / test method

It is tested whether a test object authorized for a restricted supply does not disconnect layer 3 within 30s in case of a switchover from normal operation to restricted operation. Herefore, it is tested whether the test object still reacts with STATUS INFO after the switchover with the layer-3 message STATUS INQUIRY to the test object. The display shows the result with:

- <FKT: Test passed >if the connection is kept up, or
- <FKT: Test failed >if there was a disconnection within 30s.

For the sequence of the measurement, the following selection can be made:

- External As with previous versions an external protocol tester is required; otherwise as.....
- Internal/manually After START a key is displayed with which the switchover can be triggered.
- Internal/automatically The switchover is automatically initiated by the K1403.

The TE is supplied in normal operation with an editable voltage from PS1. Following establishment of layer 3 (establishment of a connection) by the K1403, a switchover can be made to restricted operation with an editable switchover duration using the key "Switchover". Both the voltage in restricted operation and the selected current limitation can be edited. The measurement is carried out internally. The power, voltage and current are output approx. every 3 seconds. The measurement during normal operation is made in the range 0 to 230 mA, measurement during restricted operation in the range 0 to 50 mA. The terminators for the RX, TX lines of the S_0 bus can be selected in the menu field "S_0 - R".

Voltage characteristic for normal/restricted switchover

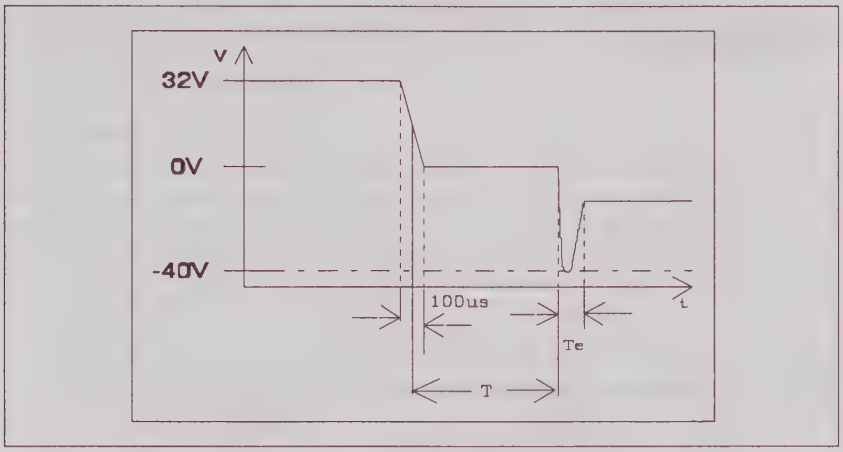


Fig. 5.7: Voltage characteristic for normal/restricted switchover

T: Switchover time

T_e: Response time of current limitation

Restricted to normal operation

(ETS §D.5.1.4.6.2)

			RANGE SELECT 0..230mA	S0-R 50Ω
MEASUREMENT (TE) SWITCHOVER TESTS	MODE RESTRICTED ---> NORMAL	CONTROL INTERNAL SWITCHOVER MANUAL	VOLTAGE (NORMAL) 32.0 V	VOLTAGE (RESTR.) 40.0V (-)

Setting parameters (MENU)

MEASUREMENT	MODE	CONTROL	RANGE SELECT	S0 - R	VOLTAGE (NORMAL)
POWER CONSUMPTION	NORMAL ---> RESTRICTED	EXTERNAL SWITCHOVER MANUAL	0 ... 230 mA	50 Ω	EDIT
CURRENT/ TRANSIENT MEASUREMENT	**RESTRICTED --->NORMAL**	INTERNAL SWITCHOVER MANUAL	0 ... 70 mA	100 Ω	LAST EDIT VALUE
CURRENT/TIME MEASUREMENT		INTERNAL SWITCHOVER AUTOM.	0 ... 38 mA		24 V
POWER START-UP TESTS			0 ... 6 mA		32 V
SWITCHOVER TESTS					
SHORT INTERRUPTION					

VOLTAGE (RESTRICTED)
EDIT
LAST EDIT VALUE
RESTRICTED 32 V
RESTRICTED 40 V

Measured quantity

Measurement of the power consumption of a test object authorized for a restricted supply and with a maximum power consumption following switchover from restricted operation to normal operation.

Test method

The TE is supplied in restricted operation with an editable voltage from PS1. A switch is made to the measuring range specified by the user approx. 3 seconds after switching on. Following activation of layer 1, a switchover can be made to normal operation with a fixed switchover duration of 100 μs using the key "Switchover". Achievement of the status F7 is indicated by a message in the display. The voltage can also be edited in normal operation. A power measurement is carried out for 500 ms following switching over. The measured values are output on the screen. A switch is made to the measuring range 0 to 230 mA at the end of the measurement. The terminators for the RX, TX lines of the S_0 bus can be selected in the menu field "S_0 - R".

Measurement (START/STOP)

The START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module Power feeding are initialized. The following status message appears in the display

`INIT/START`

The measurement subsequently starts and is indicated by

`MEASURE`

The switchover occurs after pressing the button

`SWITCHOVER`

Please note that the switchover only occurs after the output of initial measured values. If the switchover key is pressed prior to this, it will be ignored and no switchover will take place.

Presentation of results

During the measurement the results are displayed as follows

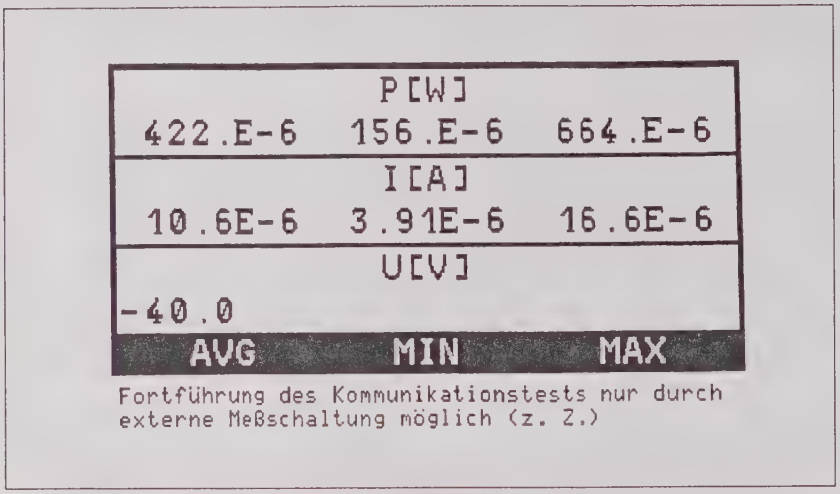


Fig. 5.8: Presentation of results for the switchover test

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.1.6 Short interruption

(ETS §D.5.1.4.3, D.5.1.4.5.X)

Interruption at TE with detector

				DISCON. TIME 500ms	S0-R 50Ω
MEASUREMENT (TE) SHORT INTERRUPTION	DISCONNECTION MODE DISCON. TE WITH DETECTOR	CONTROL INTERNAL MANUAL	STATUS Fx F4	VOLTAGE NORMAL 24.0 V	

Setting parameters (MENU)

MEASUREMENT
POWER CONSUMPTION
CURRENT/ TRANSIENT MEASUREMENT
CURRENT/TIME MEASUREMENT
POWER START-UP TESTS
SWITCHOVER TESTS
SHORT INTERRUPTION

DISCONNECTION MODE	CONTROL	STATUS Fx	DISCON. TIME	S0 - R
INTERRUPTION ON TE WITH DETECTOR	INTERNAL MANUAL	F4	EDIT	50 Ω
VOLTAGE DIPS ON TE	INTERNAL AUTOM.	F6	LAST EDIT VALUE	100 Ω
		F7	500 ms	

VOLTAGE
EDIT
LAST EDIT VALUE
24 V
32 V
NORMAL
RESTRICTED
RETURN

Interruption at TE with detector

				DISCON. TIME 500ms	S0-R 50Ω
					P.NUMBER > SUB.ADR. >
				CHANNEL SELECTION B1	INFORM. TRANS. CAPABILITY SPEECH
MEASUREMENT (TE) SHORT INTERRUPTION	DISCONNECTION MODE VOLTAGE DIPS ON TE	CONTROL INTERNAL VOLTAGE DIPS MANUAL	BASIC INTERCONN. TESTS UPSTREAM	VOLTAGE NORMAL 24.0 V	

Setting parameters (MENU)

MEASUREMENT	DISCONNECTION MODE	CONTROL	BASIC INTERCONN. TESTS	DISCON. TIME	S0 - R
POWER CONSUMPTION	INTERRUPTION ON TE WITH DETECTOR	EXTERNAL VOLT. DIPS MANUAL	UPSTREAM	EDIT	50 Ω
CURRENT/ TRANSIENT MEASUREMENT	**VOLTAGE DIPS ON TE**	INTERNAL VOLT. DIPS MANUAL	DOWNSTREAM	LAST EDIT VALUE	100 Ω
CURRENT/TIME MEASUREMENT		INTERNAL VOLT. DIPS AUTOM.		500 ms	
POWER START-UP TESTS					
SWITCHOVER TESTS					
SHORT INTERRUPTION					

VOLTAGE	INFORMATION TRANSMISSION CAPABILITY	CHANNEL	P.NUMBER > SUB.ADR. >
EDIT	SPEECH	B1	P.NUMBER
LAST EDIT VALUE	AUDIO 3.1KHZ	B2	SUB.ADR.
24 V	DATA		CLEAR
32 V	AUDIO 7KHZ		RETURN
NORMAL	VIDEO		
RESTRICTED			
RETURN			

The parameters INFORMATION TRANSMISSION CAPABILITY, CHANNEL and P.NUMBER /SUB.ADR. are only offered if the parameter CONTROL was set to INTERNAL. See also section 5.1.1.

5.1.6.1 Voltage detector

(ETS §D.5.1.4.3)

Measured quantity

Response of a TE with voltage detector on interruption of the PS1 voltage.

Test method

The test object is supplied with an editable DC voltage from the PS1. At the same time, the test object is set to a status entered by the user. Once this status has been reached, the voltage interruption is carried out automatically for the set duration. The response of the layer 1 protocol is documented on the screen. P, I and U are output approx. every second. The measurement is made in the range 0 to 230 mA.

Presentation of results

During the measurement the currently measured values P[W], I[A] and U[V] are displayed. At the end of the test, „Test ok" / „Test failed" shows if the set status was reached or maintained.

5.1.6.2 Voltage interruptions

(ETS §D.5.1.4.5.X)

Measured quantity

A test is carried out to establish whether a TE clears layer 3 if there is an interruption in the PS1 voltage.

Test method / Presentation of results

It is tested whether an test object does not disconnect a layer-3 connection within 30s after an interruption of the PS1 for 5ms. This is carried out by sending the STATUS INQUIRY message. The display shows the result with:

- <FKT: Test passed >if the connection is kept up, or
- <FKT: Test failed >if there was a disconnection within 30s

For the sequence of the measurement, the following selection can be made:

- External — As with previous versions an external protocol tester is required; otherwise as.....
- Internal/Manually — After START a key is displayed with which the interruption can be triggered.
- Internal/automatically — The interruption is automatically initiated by the K1403.

The test object is provided with an editable DC voltage from the PS1. Following establishment of a layer 3 by the protocol tester, a voltage interruption with an editable duration can be executed by pressing the key "Interrupt voltage".

P, I and U are output approx. every second. The measurement is made in the range 0 to 230 mA.

Interruption timing

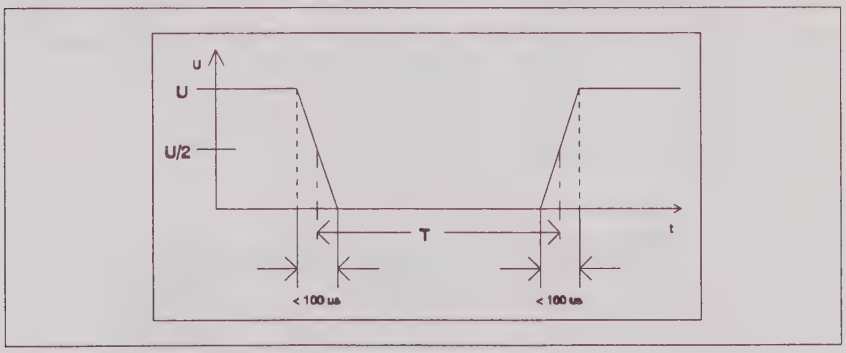


Fig. 5.9: Interruption timing

Measurement (START/ STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the power feeding module are initialized. The following status message appears in the display

`INIT/START`

The measurement subsequently starts and is indicated by

`MEASURE`

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.2 Power feeding conditions NT

5.2.1 Power output

(ETS §E.5.1.X)

				MIN. LOAD CURRENT 0.25 mA	CURRENT CHANGE ΔI 0.25 mA
				MAX. LOAD CURRENT 135.0 mA	DURATION OF ΔI 0.1 s
				AVERAGING TIME 50 ms	S0-R 100 Ω
					INTERFACE 0
MEASUREMENT (NT) NOR/REST.: POWER OUTPUT	POWER FEEDING PS1			MINIMUM VOLTAGE 34 V	

Setting parameters (MENU)

MEASUREMENT	POWER FEEDING	MIN. LOAD CURRENT	CURRENT CHANGE ΔI	MAX. LOAD CURRENT	DURATION OF ΔI
NOR//REST. POWER OUTPUT	PS1	EDIT	EDIT	EDIT	EDIT
	PS2	LAST EDIT VALUE	LAST EDIT VALUE	LAST EDIT VALUE	LAST EDIT VALUE
		0.25 mA	0.25 mA	135 mA	0.1 s
			1.00 mA	240 mA	1.0 s
			10.00 mA		

AVERAGING TIME	S0-R	MINIMUM VOLTAGE	INTERFACE
50 ms	50 Ω	EDIT	EDIT 0 .. 15
100 ms	100 Ω	LAST EDIT VALUE	
		34 V (-15%)	

Measured quantity

Measurement of maximum power output of an NT.

Test method

After starting the measurement, the minimum current load is set. Then the value of the current sink is increased step by step up to the maximum value within fixed time intervals. The minimum and maximum loads as well as current changes and time intervals are editable. If you select PS2 as supply, connect the NT to the sockets U1 and U2 via an application circuit.

For each load setting, the voltage and current (sampling frequency 500 Hz) are measured, the power is calculated by averaging it over 50 ms or 100 ms and the *minimum value* of the power output is obtained. Before each increase in the load, this minimum value is compared with the previously recorded power value. The larger value is processed further. After the maximum current load has been reached, the maximum value of the power output calculated in this way as well as the corresponding current and voltage values are displayed on the screen. Current measured values are output approx. every second. If the NT supplies in restricted operation, a minus sign appears before the voltage value in the display. After that a new measurement cycle is carried out. If you select PS1 as supply, the internal resistance of the S_0 transmitter is 3.5Ω, which is taken into consideration for the calculations.

If an NT voltage lower than half of the minimum voltage set is recorded after activating the measurement, an error message is output and the measurement is not started. The measurement is aborted if the NT voltage falls below the minimum voltage set during the measurement of the measured quantities.

The value displayed in the menu field Interface is output to the socket X6/I0-I3 (pin2 - pin5) and serves to control and decode external hardware.

External interface

Ix	Function	
I_0	Output of value edited by the user (in binary code)	2^0
I_1		2^1
I_2		2^2
I_3		2^3
I_5	Not in use	

Presentation of results

- Approx. every second: current P, U, I
- Once/measuring cycle: a) maximum power with U_{pmax} and I_{pmax}
  b) number of measuring cycles

Measuring accuracy

see *Appendix* "Technical data for the power feeding conditions".

5.2.2 Switchover test

(ETS: §E.5.1.3)

				LOAD CURRENT NORMAL 100.0 mA (4 TEs)	LOAD INTERNAL
					S0-R 100Ω
					INTERFACE 0
MEASUREMENT (NT) NOR/REST.: SWITCHOVER T.	SWITCHOVER NORMAL --> RESTRICTED				

Setting parameters (MENU)

MEASUREMENT	SWITCHOVER	LOAD CURRENT NORMAL	LOAD	S0-R	INTERFACE
NOR/REST. SWITCHOVER T.	NORMAL --> RESTRICTED	EDIT	INTERNAL	50Ω	EDIT 0 .. 15
	RESTRICTED --> NORMAL	LAST EDIT VALUE	EXTERNAL	100Ω	
		25 mA (1TE)			
		100 mA (4TEs)			
		200 mA (8TEs)			

Measured quantity

Measurement of NT switchover time from 34 V in normal operation to -34 V in restricted operation and vice versa.

Test method

For this measurement, the test object is loaded with a 3.8 kΩ resistor in restricted operation. In normal operation, the NT is loaded with current sink which is connected in parallel to the 3.8 kΩ resistor. The 10.5 mA current flowing through the resistor during a 40 V S_0 voltage is taken into account by the current sink setting. The means, however, that at a NT voltage of 36 V, the load current would be approx. 1 mA (4 V/3.8 kΩ) too low. If the S_0 voltage deviates greatly from 40 V in normal operation, this must be taken into account by the current sink setting (1.05 mA/4 V).

If the setting parameter "External load" has been selected, an external load can be connected to sockets U1 and U2. Please pay attention to the polarity though.

The NT is loaded with the current edited by the user in normal operation and delivers 34 V (-34V). After measurement has begun, signal I5 of the external interface, which can be used to drive a hardware for switch-on/switchover of the NT line voltage, is set from high to low. The measurement begins when the NT connected to the K1403 is in normal (restricted) operation.

Signal I5 of the external interface, which can be used to drive a hardware for switchover of the NT line voltage, changes (restricted operation = LOW, normal operation = HIGH) approx. 1 second after the current load is applied. At the same time on the screen there is an entry "PWR:SWITCH OVER/ON".Measurement of the switchover time begins once the S_0 voltage drops below 34 V. The switchover time is measured for a period of 1 second (see diagram). If the switchover is not complete within this 1 second, the message "∞" is output. There is a delay of approx. 90 µs at the beginning of measurement.

The actual voltage, current and power output values for the NT are entered in the result field approx. once a second. However, with the "External load" setting, only the voltage value is correct.

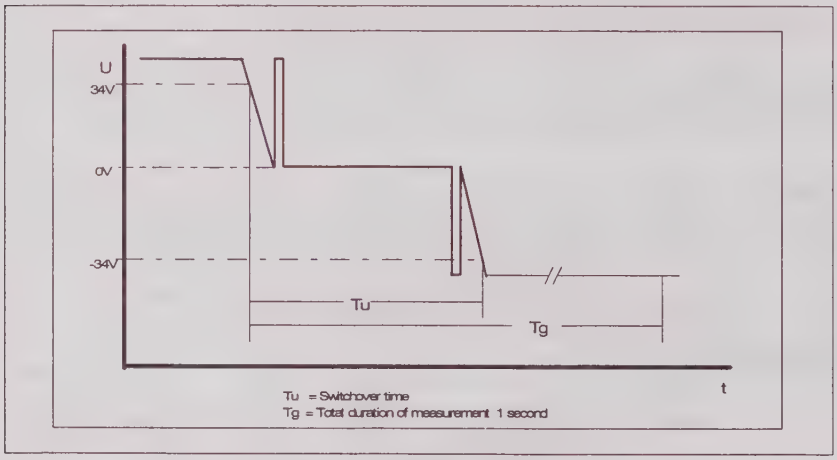


Fig. 5.21: Example of a switchover from normal to restricted operation

The value set in the menu field "Interface" is output to socket X6/I0-I3 (pin 2 - pin 5) and drives and decodes external hardware.

External interface

Ix	Function	
I_0	Output of value edited by the user (in binary code)	2^0
I_1		2^1
I_2		2^2
I_3		2^3
I_5	Normal operation : High Restricted operation : Low	

External load

Connection to sockets U_1(-) and U_2(+). The polarity for normal operation is given in brackets.

Presentation of results

- Approx. every second: current P, U, I
- Once: switchover time

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.2.3 Switch-on response

(ETS: §E.5.1.6)

				LOAD CURRENT T < 100 ms 180.0 mA (4 TEs)	S0-R 100Ω
				LOAD CURRENT T > 100 ms 100.0 mA (4 TEs)	INTERFACE 0
				AVERAGING TIME 50 ms	
MEASUREMENT (NT) NOR: SWITCH-ON RESPONSE.					

Setting parameters (MENU)

MEASUREMENT	LOAD CURRENT T < 100 ms	LOAD CURRENT T > 100 ms	AVERAGING TIME	S0-R	INTERFACE
NOR: SWITCH-ON RESPONSE	EDIT	EDIT	50 ms	50 Ω	EDIT 0 .. 15
	LAST EDIT VALUE	LAST EDIT VALUE	100 ms	100 Ω	
	45 mA (1TE)	25 mA (1TE)			
	180 mA (4TEs)	100 mA (4TEs)			
	360 mA (8TEs)	200 mA (8TEs)			

Measured quantity

The test checks whether the NT can supply a current of n x 45 mA for 100 ms without the voltage dropping below 30 V following switch-on in normal operation or switchover from restricted to normal operation. 'n' represents the number of TEs. The NT must be able to output (n x 1) Watt at the end of these 100 ms with a voltage of > = 34 V.

Test method

To guarantee a correct measuring procedure, the output of an error information is done if the NT is in normal mode after starting the measurement. The NT being active or in restrictive mode, signal I5 of the external interface, which can be used to drive a hardware for switch-on/switchover of the NT line voltage, is set from low to high. The measurement begins when the NT connected to the K1403 is in normal operation. The NT is loaded with the value edited by the user for the current sink (setup parameter: LOAD CURRENT T < 100 ms) in normal operation. Once the S_0 voltage has exceeded 30 V, the S_0 voltage is measured with a 500 Hz sampling frequency for a period of 100 ms. Once this is complete, the load sink (setup parameter: LOAD CURRENT T > 100 ms) set by the user is applied and the S_0 voltage measured for another second. The first measuring point is detected 2 ms after the load switchover.

6 voltage values are output:

- The minimum voltage
- The maximum voltage
- The averaged minimum voltage for each time interval

  {0 < t < 100 ms} after the 30 V voltage has been exceeded as well as
  {0 < t < 1 s} after the load change.

The actual voltage, current and power output values for the NT are also output approx. once a second.

External interface

Ix	Function	
I_0	Output of value edited by the user (in binary code)	2^0
I_1		2^1
I_2		2^2
I_3		2^3
I_5	Switchover from low to high	

Presentation of results

- Approx. every second: current P, U, I
- Once for

  0 ms < t <100 ms U_{Min} , U_{Max}, $U_{MinØ}$
  0 s < t < 1 s U_{Min} , U_{Max}, $U_{MinØ}$

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.2.4 Overload in restricted operation - test A: response to short circuit

(ETS: §E.5.1.4.1)

				AVERAGING TIME 50 ms	S0-R 100 Ω
					INTERFACE 0
MEASUREMENT (NT) RESTRICTED (A): AT SHORT CIRCUIT					

Setting parameters (MENU)

MEASUREMENT	AVERAGING TIME	S0-R	INTERFACE
RESTRICTED (A): AT SHORT CIRCUIT	50 ms	50 Ω	EDIT 0 .. 15
	100 ms	100 Ω	

Measured quantity

This test checks whether a NT can output a 9-mA short-circuit current for a duration of one second, one second after switchover from normal to restricted operation.

Test method

The measurement begins when the NT connected to the K1403 is in normal operation (otherwise error message). Once measurement has begun, signal I5 of the external interface is switched over from high to low level. This allows you to perform an external switchover with which the NT line voltage can be switched off. At the same time "PWR SWITCHOVER/ON" is output on the screen. Following the switchover from normal to restricted operation, the measurement begins and the NT is short-circuited for 1 second. The current is then measured and evaluated with a 500 Hz sampling frequency for 1 second. The minimum and maximum current and minimum current values averaged over 50 or 100 ms measured during this period are entered in the result field. The actual voltage, current and power output values are issued approx. once a second.

External interface

Ix	Function	
I_0	Output of value edited by the user (in binary code)	2^0
I_1		2^1
I_2		2^2
I_3		2^3
I_5	Measurement in restricted operation: Low level	

Presentation of results

- Approx. every second: current P, U, I
- Once: I_{Max}, I_{Min}, $I_{Min\varnothing}$

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.2.5 Overload in restricted operation - test B: reduction of current load after short circuit

(ETS: §E.5.1.4.2)

				1 V STEP DURATION 0.2 s	S0-R 100 Ω
				AVERAGING TIME 50 ms	INTERFACE 0
MEASUREMENT (NT) RESTRICTED (B): AT SHORT CIRCUIT					

Setting parameters (MENU)

MEASUREMENT	1 V STEP DURATION	AVERAGING TIME	S0-R	INTERFACE
RESTRICTED (B): AT SHORT CIRCUIT	EDIT	50 ms	50 Ω	EDIT 0 .. 15
	LAST EDIT VALUE	100 ms	100 Ω	
	0.2 ms			

Measured quantity

This test checks whether a NT can output an 11 mA current at -34 V in restricted operation if the load is reduced after a short circuit.

Test method

With this measuring mode, the NT is connected to a voltage source which is able to absorb current. The measurement requires that the test object have a voltage >34 V (restricted operation) at the K1403, otherwise an error message is issued at the start. Once the measurement has begun, the S_0 voltage is increased in 1 V steps starting with 0 V at fixed intervals which can be edited by the user. At 34 V, the current is measured with a 500 Hz sampling frequency. The following is output on the screen:

- The minimum current averaged over 50 or 100 ms and
- the corresponding voltage value.

The actual voltage, current and power output values of the NT are issued approx. once a second.

External interface

Ix	Function	
I_0	Output of value edited by the user (in binary code)	2^0
I_1		2^1
I_2		2^2
I_3		2^3
I_5	Measurement in restricted operation: Low level	

Presentation of results

- Approx. every second: current P, U, I
- Once: $I_{Min\varnothing}$, $U_{\varnothing}$

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.2.6 Overload in restricted operation - test C: increase of current load over nominal load

(ETS: §E.5.1.4.3)

				LOAD CURRENT AT START 10.5 mA	
				DURATION OF ΔI 0.2 s	S0-R 100 Ω
				AVERAGING TIME 50 ms	INTERFACE 0
MEASUREMENT (NT) RESTRICTED (C): AFTER NOMINAL LOAD					

Setting parameters (MENU)

MEASUREMENT	LOAD CURRENT AT START	DURATION OF ΔI	AVERAGING TIME	S0-R	INTERFACE
RESTR. (C): AFTER NOM. LOAD	EDIT	EDIT	50 ms	50 Ω	EDIT 0 .. 15
	LAST EDIT VALUE	LAST EDIT VALUE	100 ms	100 Ω	
	10.5 mA	200 ms			
		1 s			

Measured quantity

This test checks whether a NT can output an 11 mA current at 34 V in restricted operation if the load is increased over the nominal load (420 mW).

Test method

The measurement begins when a NT with a voltage >34 V (restricted voltage) has been detected at the K1403 (otherwise an error message is issued). The start load is set at the beginning of the measurement by a current sink. The load is increased in 100 μA steps to a maximum 20 mA. The start load and time intervals can be edited by the user. The current and voltage averaged over 50 or 100 ms are measured with each current load. Two pairs of values are output on the screen:

- The voltage value at the preset 11 mA load
- The last measured voltage value before going below 34V restricted voltage with its corresponding current value. If the value with maximum load of the restricted voltage is not going below 34 V, the last measured pair of values (current and voltage) are output on the screen.

"∞" signifies that no measured values were attained.

The actual voltage, current and power output values are issued approx. once a second.

External interface

Ix	Function	
I_0	Output of value edited by the user (in binary code)	2^0
I_1		2^1
I_2		2^2
I_3		2^3
I_5	Measurement in restricted operation: Low level	

Presentation of results

- Approx. every second: current P, U, I
- Once: S_0 voltage = measured value / S_0 current = 11 mA
  S_0 voltage ≥ -34 V / S_0 current = measured value

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.2.7 Overload in restricted operation - test D: capacitive load after short circuit

(ETS: §E.5.1.4.4)

				LOAD CAPACITY 100 µF	LOAD INTERNAL
				DURATION OF SHORT CIRCUIT 1800 s	S0-R 100 Ω
					INTERFACE 0
MEASUREMENT (NT) RESTRICTED (D): AFTER SHORT CIRCUIT CAP.					

Setting parameters (MENU)

MEASUREMENT	LOAD CAPACITY	DURATION OF SHORT CIRCUIT	LOAD	S0-R	INTERFACE
RESTR. (D): AFTER SHORT CIRCUIT CAP.	EDIT	EDIT	INTERNAL	50 Ω	EDIT 0 .. 15
	LAST EDIT VALUE	LAST EDIT VALUE	EXTERNAL	100 Ω	
	100 µF	10 s			
		1800 s			

Measured quantity

This test checks whether the NT loads up a 100µF capacity to 34 V (restricted voltage) within 10 seconds after a short circuit lasting 30 minutes, whereby the restricted voltage must increase from 1 V to 34 V within 1.5 secs.

Test method

With this measuring mode, the user has the option of connecting an external load to sockets U1 and U2. Please pay attention to the polarity. If EXTERNAL LOAD is set, the externally connected load is applied. With INTERNAL LOAD, the internally simulated and editable capacity is selected.

The measurement begins once a NT with a voltage >34V (restricted voltage) is connected to the K1403. The NT connected to the K1403 is then short-circuited for a time interval which can be edited by the user. After the short circuit, the NT loads up the internal or external load, whereby the S_0 voltage is measured in 1 ms time reference. The following is output on the screen:

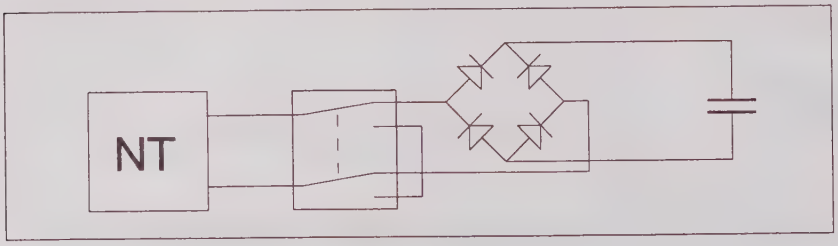
- The time from the end of the short circuit to the time when the voltage exceeded the 1 V threshold (restricted voltage) and
- the time from 1 V to the time when the voltage exceeded the 34 V threshold (restricted voltage).

If the voltage of the NT doesn´t read the 1V threshold in a time at 20 sec. (normal voltage) or the 34V threshold in a time at 3 sec. the output on the screen is "∞".

When LOAD INTERNAL has been selected, the circuitry as described by ETSI, will be disconnected from the IUT, when the results have been displayed. The measurement will be continued for observation. The IUT is subsequently connected to a low-resistive current consuming voltage source with appr. 34 V. The current value which is cyclically updated in the display thus represents the value of the NT current limitation. . After STOP the IUT is disconnected from the voltage source.

Once the measurement is complete, the actual voltage, current and power output values of the NT are issued approx. once a second. However, if "External load" is set, only the voltage value is correct.

The following circuit is simulated with the INTERNAL LOAD setting (block diagram):



External interface

Ix	Function	
I_0	Output of value edited by the user (in binary code)	2^0
I_1		2^1
I_2		2^2
I_3		2^3
I_5	Measurement in restricted operation: Low level	

External load

Connection to sockets U_1(-) and U_2(+). The polarity for normal operation is given in brackets.

Presentation of results

- Approx. every second: current P, U, I
- Once: $T_{(0\ V\text{-}1\ V)}$
  $T_{(1\ V\text{-}34\ V)}$

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.2.8 Requirements of type "a" NTs

(ETS: §E.5.1.5)

				LOAD CURRENT 60.0 mA (4 TEs)	LOAD INTERNAL
				LOAD CAPACITY 400 µF (4 TEs)	S0-R 100 Ω
				DURATION OF SHORT CIRCUIT 1800 s	INTERFACE 0
MEASUREMENT (NT) NOR: TEST TYPE "a" NT					

Setting parameters (MENU)

MEASUREMENT	LOAD CURRENT (4TEs)	LOAD CAPACITY (4TEs)	DURATION OF SHORT CIRCUIT	LOAD	S0-R	INTERFACE
NOR: TEST TYPE "a" NT	EDIT	EDIT	EDIT	INTERNAL	50 Ω	EDIT 0 .. 15
	LAST EDIT VALUE	LAST EDIT VALUE	LAST EDIT VALUE	EXTERNAL	100 Ω	
	15 mA (1TE)	100 µF (1TE)	10 s			
	60 mA (4TEs)	400 µF (4TEs)	1800 s			
	120 mA (8TEs)	800 µF (8TEs)				

Measured quantity

This test checks whether a NT loads up a load from (n x TE) models to 34 V within 10 seconds following a short circuit of 30 minutes in length in normal operation. The voltage must also increase from 1 V to 34 V within 350 ms. In this case, "n" refers to the number of TEs.

Test method

With this measuring mode, the user has the option of connecting an external load to sockets U1 and U2. Please pay attention to polarity. If EXTERNAL LOAD is set, the externally connected part of the circuit is applied. With the INTERNAL LOAD setting, the internally simulated part of the circuit (see diagram), to which the capacity and current sink values can be edited, are selected.

The measurement begins once a NT with a voltage >34V (normal voltage) is connected to the K1403. The NT connected to the K1403 is then short-circuited for a time interval which can be edited by the user. After the short circuit, the NT loads up the internal or external load, whereby the S_0 voltage is measured in 1 ms time reference.

The following is output on the screen:

- The time from the end of the short circuit to the time when the voltage exceeded the 1 V threshold (normal voltage) and
- the time from 1 V to the time when the voltage exceeded the 34 V threshold (normal voltage).

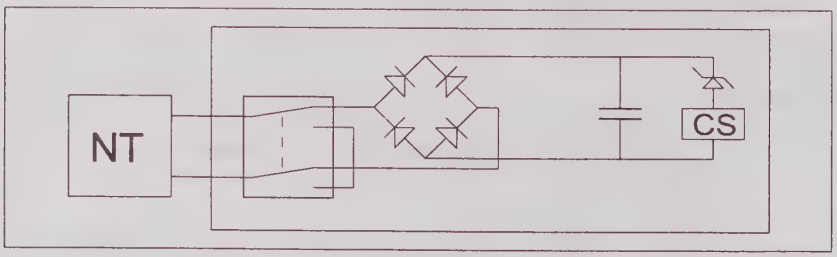
If the voltage of the NT doesn't read the 1V threshold in a time at 20 sec. (normal voltage) or the 34V threshold in a time at 3 sec. the output on the screen is "∞".

When LOAD INTERNAL has been selected, the circuitry as described by ETSI, will be disconnected from the IUT, when the results have been displayed. The measurement will be continued for observation. The IUT is subsequently connected to a low-resistive current consuming voltage source with appr. 34 V. The current value which is cyclically updated in the display thus represents the value of the NT current limitation. . After STOP the IUT is disconnected from the voltage source.

After the measurement the voltage, current and power output values are updated approximately once per second. With the setting LOAD INTERNAL only the voltage is correct.

The voltage drop on the S0-transformers (source resistance ≈ 3Ω) is not compensated during the voltage measurement

The following circuit is simulated with the INTERNAL LOAD setting (block diagram):



External interface

Ix	Function	
I_0	Output of value edited by the user (in binary code)	2^0
I_1		2^1
I_2		2^2
I_3		2^3
I_5	Measurement in normal operation: High level	

External load

Connection to sockets U_1(-) and U_2(+). The polarity for normal operation is given in brackets.

Presentation of results

- Approx. every second: current P, U, I
- Once: $T_{(0\ V\text{-}1\ V)}$
  $T_{(1\ V\text{-}34\ V)}$

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

5.2.9 Current change due to connection of a TE

				LOAD CURRENT AT START 90.0 mA (3 TEs)	S0-R 100 Ω
				AVERAGING TIME 50 ms	INTERFACE 0
MEASUREMENT (NT) NOR: CONNEC-TION OF 1 TE					

Setting parameters (MENU)

MEASUREMENT	LOAD CURRENT AT START	AVERAGING TIME	S0-R	INTERFACE
NOR: CONNECTION OF 1 TE	EDIT	50 ms	50 Ω	EDIT 0 .. 15
	LAST EDIT VALUE	100 ms	100 Ω	
	30 mA (1TE)			
	90 mA (3TEs)			
	210 mA (7TEs)			

Measured quantity

This test checks whether a NT that supplies a current of (n-1) x 30 mA in normal operation can additionally supply a current of 50 mA for a period of 100 ms and then n x 30 mA without the voltage falling below the 34 V threshold. "n" represents the number of TEs.

Test method

The measurement begins when a NT with a voltage of >34V (normal voltage) is connected to the K1403. Once the measurement has begun, a start load, which can be adjusted by the user, is set. After measuring a S_0 voltage of >34 V (sampling frequency: 500 Hz) for approx. 3 seconds, the NT is loaded with an additional current of 50 mA for 100 ms followed by 30 mA.

The minimum, maximum and minimum voltage averaged over 50 or 100 ms which were measured

- during the period 0<T<100 ms and
- during the period 0<T<1000 ms

are output on the screen.

The actual voltage, current and power output values of the NT are issued approx. once a second.

External interface

Ix	Function	
I_0	Output of value edited by the user (in binary code)	2^0
I_1		2^1
I_2		2^2
I_3		2^3
I_5	Measurement in normal operation: High level	

Presentation of results

- Approx. every second: current P, U, I, minimum voltage
- Once: 0<t<100 ms: U_{Min}, U_{Max}, $U_{Min\varnothing}$
  0 ms<t<1000 ms: U_{Min}, U_{Max}, $U_{Min\varnothing}$

Measuring accuracy

See *Appendix* "Technical data for the power feeding conditions".

6 Remote control of the K1403

Before operating the unit under remote control via the IEC bus, the device address (default setting address = 17) must be checked or set in the basic menu by selecting the field SETUP. Addresses may be set between 1 and 30. If a new address is selected, the unit must be switched off and on in order to initialize the IEC bus interface with this address. If several devices are connected to the IEC bus, a different address must be set for each one.

Remote control operation is indicated by a "**R**" in the display.

The maximum permissible isolating voltage between the measurement sockets BU6 and protective ground or BU7 and protective ground is 100 V.

When using a non-isolated IEC bus card, the electrical isolation between internal ground and protective ground is canceled.

Special settings via IEC

If "upstream" and "downstream" was selected for the basic interconnection test, it is possible to use a user-defined SETUP string in layer 3. Furthermore, a call number (Called Party Number) and an extension number (Called Party Subaddress) can be programmed.

The special settings via IEC are not available until SW Version 5.0.

User-defined SETUP string

With the IEC command L3-SETUP, a SETUP string with up to 510 byte for the basic interconnection test can be programmed. This remains saved until the device is switched off.

L3_SETUP n,m_1,.....,m_n	**n={1..510}**	: Length of the SETUP string in decimal display (e.g.: FF=255)
	m_n	: Elements of the SETUP string in decimal display

A space must be input between the command and the length specification n. The SETUP string programmed in this way is only used if the parameter INFORMATION TRANSMISSION CAPABILITY is set to USER-DEFINED.

Called Party Number

With the IEC command L3-CALLED_P, a called party number with up to 20 digits can be entered for the basic interconnection test in layer 3. This number remains saved until the device is switched off.

L3_CALLED_P p_1,.....,p_k	**p={0..9}**	: Digit of called party number in ASCII representation, left aligned
	k={1..20}	

A space must be entered between the command and the first digit. The called party number programmed in this way is not used if the parameter INFORMATION TRANSMISSION CAPABILITY was set to USER-DEFINED.

Called Party Subaddress

With the IEC command L3-CALLED_SUB, a called party subaddress with up to 20 digits can be entered for the basic interconnection test in layer 3. This number remains saved until the device is switched off.

L3_CALLED_SUB s_1,.....,s_k	**s={0..9}**	: Digit of called party subaddress in ASCII representation, left aligned
	k={1..20}	

A space must be entered between the command and the first digit. The called party subaddress programmed in this way is not used if the parameter INFORMATION TRANSMISSION CAPABILITY was set to USER-DEFINED.

6.1 Command and parameter syntax

All the functions of the unit can be remotely controlled via the IEC interface. All the device settings and feedbacks are triggered by character strings. The command names are based on the corresponding functions. In order to indicate the end of message (EOI) when transmitting a command to the unit, the token LF (0A hexadecimal) has to be used. The device also uses this character for the data output.

For example the command `START`

triggers the start of a measurement on the device.

All command names which effect the interrogation of a device setting are terminated by a '?'.

The request command `RUNNING?`

for example can be used to check the current status of the measuring cycle.

A command consists of a header (command name) and one or more numerical parameters where applicable. The header must be entered in upper-case letters. At least one space must be entered between the command header and the parameters. If there are several parameters, they are separated by commas (' , ').

Example: `'TIME 12,00,00'`

Numerical parameters

Numerical parameters may be entered as integers, fixed-point numbers or floating-point numbers with or without exponents. The exponent may comprise up to two digits, the exponent symbol 'E' must be in upper case. A space may be entered before and after the exponent symbol. Plus signs may be omitted.

Example: Parameter to be represented: `12.5` (twelve + decimal fraction)

```
'12.5'
'0012.5'
'1.25E1'
'+1.25 E+01'
```

Strings of commands

It is possible to transmit several commands in one string. The commands are separated by a semicolon (;). Spaces may be entered before and after the semicolon.

Example: `'TIME? ; RUNNING? ; START'`

Request commands

All request commands are terminated by a '?'. The device sends a feedback to the controller as a reaction to a request command. When operating with an IEC interface, the status byte can be read or a serial poll carried out to determine whether a device message is ready. Bit 4 (=16) is set in the status byte in this case (MAV, Message AVailable).

Input errors

Incorrect inputs and commands which cannot be executed generate an error message. This causes a certain bit to be set in an event register. The controller can then read the register to determine the type of error which has occurred.

6.2 Overview of commands

The instruction set of the device is described in the following. The commands can be entered directly over the keyboard in the form printed below.

6.2.1 IEC standard commands

`*CLS`	Clears the status byte and the event registers
`*ESE`	Sets the event status enable register
`*ESE?`	Reads the event status enable register
`*ESR?`	Reads the event status register
`*PRE`	Sets the parallel poll enable register
`*PRE?`	Reads the parallel poll enable register
`*SRE`	Sets the service request enable register
`*SRE?`	Reads the service request enable register
`*STB?`	Reads the status byte
`*RON`	Remote control on (R appears in the upper left corner of the display)
`*ROF`	Remote control off
`*IST?`	Reads the parallel request bit
`*OPC`	Sets Operation-complete Flag
`*OPC?`	Sets Operation-complete-Reaction
`ERAE`	Sets event enable register A
`ERAE?`	Reads event enable register A
`ERA?`	Reads event register A

ERBE	Sets event enable register B
ERBE?	Reads event enable register B
ERB?	Reads event register B
*IDN?	Interrogates the device identification
*LRN?	Interrogates the parameter settings

6.2.2 Setting commands

TIME	Sets the clock in K1403
TIME?	Interrogates the clock in K1403
DATE	Sets the date in K1403
DATE?	Interrogates the date in K1403
LANGUAGE	Sets the language of the device
LANGUAGE?	Interrogates the language set in the device
IEEE_ADDRESS	Sets the IEC bus address
IEEE_ADDRESS?	Interrogates the IEC address settings

6.2.3 Measuring commands

START	Starts measurement
STOP	Stops measurement
RUNNING?	Interrogates the status of the device during measurement
MEASURE	Sets the parameters for measurement
MEASURE?	Interrogates the measurement parameter settings
ART_LINE	Sets the parameter settings for artificial line
ART_LINE?	Interrogates the parameters for artificial line
TRACE?	Reads out the ONLINE measuring results
CLEAR_TRACE	Clears the trace memory
RESULT?	Reads out the results after measurement has been stopped
READ_STATUS?	Reads out the status information from the status ring list
CLEAR_STATUS	Clears the status ring list
UPDATE	Triggers an action (specific to measuring mode)
PRINTOUT 0	Outputs a hardcopy via RS 232

6.3 Command description

The operation and possible parameters of the various IEC device commands are described in greater detail in this section. The device **must** have completed the initialization which takes place after switching on!

6.3.1 IEC standard commands

*CLS

Clears the status byte and the event registers.

`*ESE, *ESE?, *ESR?`

See section: "Event and status registers".

`*PRE, *PRE?`

See section: "Event and status registers".

`*SRE, *SRE?, *STB?`

See section: "Event and status registers".

`*RON, *ROF`

Command: `*RON`

The command '`*RON`' activates operation of the device in remote control mode.

(An R appears in the top left corner of the screen)

Command: `*ROF`

The command '`*ROF`' deactivates operation of the device in remote control mode.

(The R in the top left corner of the screen disappears)

`*IST?`

See section: "Event and status registers".

`*ERA?`

See section: "Event and status registers".

`*ERBE, ERBE?, *ERB?`

See section: "Event and status registers".

*IDN?

Command: *IDN?

The command '*IDN?' causes the identification character string of the device to be output.

It looks like this:

SIEMENS,7KK1403,rrttuuvvwwxxyyzz.aabbccddeeffFFgghhHH

Character	Meaning		Character	Meaning
rr	Hardware version Main computer		aa	Firmware version Main computer
ss	Hardware version ANALOG1		bb	Firmware version ANALOG1
tt	Hardware version ANALOG2		cc	Firmware version ANALOG2
uu	Hardware version POWER		dd	Firmware version POWER
vv	Hardware version MEASURING PANEL		ee	xx (No firmware)
ww	Hardware version FUNCTIONAL TESTS (1) (OPT)		ff	Firmware version FUNCT1
xx	Hardware version FUNCTIONAL TESTS (2) *) (OPT)		FF	Firmware version FUNCT2
yy	Hardware version ARTIFICIAL LINE (OPT)		gg	xx (No firmware)
zz	Hardware version JITTER (OPT)		hh	Firmware version JITTER (1)
			HH	Firmware version JITTER (2)

*) The hardware version is indicated for each computer. It is, however, only one module.

If no (optional) modules are fitted, this is indicated with a '-'.

6.3.2 Setting commands

TIME

Command: `TIME hh,mm,ss`

where hh = hours, mm = minutes, ss = seconds;

The command '`TIME`' sets the real-time clock in K1403. The time can currently only be read out in connection with the command `'RESULT? 1'`.

Example:
```
TIME 15,46,0
TIME?   -->  +15,+46,+0
```

DATE

Command: `DATE dd,mm,yy`

where dd = days, mm = months, yy = years;

The command '`DATE`' sets the date of the real-time clock in K1403. The date can currently only be read out in connection with the command `'RESULT? 1'`.

Example:
```
DATE 19,03,93
DATE?   -->  +19,+3,+93
```

LANGUAGE

Command: `LANGUAGE` <Index> where

<Index> = 0 : English;

<Index> = 1 : German;

The command '`LANGUAGE`' sets the device language in the K1403.

Example:
```
LANGUAGE 1
LANGUAGE?   -->  +1
```

IEEE_ADDRESS

The device address of the K1403 can be changed by entering the command `'IEEE_ADDRESS'`.

The device only responds to the new address after it has been switched off and on again!

Example:
```
IEEE_ADDRESS 12
IEEE_ADDRESS?   -->  +12
```

6.3.3 Measuring commands

Starting a measurement

Command: `START`

The command 'START' sets the device to the measuring status. The command 'MEASURE' should first be executed.

Artificial line option parameters

Command: `ART_LINE`

Example: `ART_LINE 0,0,0,0,1,0,0,0,2,0,0,0` defines a line configuration of the artificial line for a specific measuring mode.

Interrogating the line configuration of the artificial line option

Command: `ART_LINE?`

The request command `'ART_LINE?'` reads as a result the parameters of the line configuration just set.

Example: `ART_LINE? --> 0,0,0,0,1,0,0,0,2,0,0,0`

Joint usage of `MEASURE` and `ART_LINE`

The artificial line option may only be used with certain K1403 measuring modes. If measuring modes are changed, the K1403 menu manager will change certain line parameters accordingly. The `MEASURE` command must therefore be entered first and then the relevant `ART_LINE` command in order to produce valid parameter settings.

Interrogation of ON-LINE results during measurement

Command: `TRACE?`

When the device is measuring under remote control, the measuring results are written to an internal trace buffer. The relevant bit is set in event register A (TAV = Trace AVailable). This data can be obtained from the device using the TRACE? command. A binary data format is used for the measuring results:

Data format: ARBITRARY BLOCK PROGRAM DATA (ANSI/IEEE Std 488.2)

<#> < XA> <XB1> <XB2>... <XBn> <Byte 1> <Byte 2>.... <Byte n>

where:

<#>	:	Preamble
<XA>	:	Length of length data in bytes (in ASCII code)
<XB1>..<XBn>	:	Number of data bytes (in ASCII code)
<Byte 1>	:	Number of measuring results in the trace buffer (in binary code)
<Byte 2>..<Byte n>.	:	Measuring results of the measuring mode in question

MEASURING DATA FORMAT starting with < Byte 2>

No.	Type	Meaning
1	BYTE	Result or Trace: Trace = 0 ; Result = 1
2	BYTE	IEC address (0 - 31)
3, 4	WORD	Length of header in BYTES (here 15)
5, 6	WORD	Length of measuring results after header in bytes (structure of measuring results depends on measuring mode)
7	BYTE	Not used
8	BYTE	Number of data blocks for a complete "measuring curve" (only with measuring modes Impedance, Unbalance)
9	BYTE	Current data block: (only with measuring modes Impedance, Unbalance)
10	BYTE	Internal format coding, e.g. 0: Graphical results 1: Numerical results 2: ASCII string
11	BYTE	Conformance byte Evaluation whether the measuring result is within the limits of tolerance. The test required for this depends on the measuring mode (see description of measurement data structure)
12....15	BYTE	RESERVE
16.....	BYTE	Measuring results with length according to nos. 5, 6 *****MEASURING RESULTS********

Data types:

BYTE = 8 bit (MSB.....LSB)

WORD = 16 BIT (LOW BYTE, HIGH BYTE)

Almost every measuring mode provides measuring results in different lengths and formats. The 15-byte header serves to inform the user about the characteristics of the measuring results. However, only those parameters which are useful are set.

BYTE 1

The evaluation of the number of measuring results in the trace buffer makes it possible for the user to monitor an 'ONLINE' application with respect to timing. If <BYTE 1> increases, the device registers measuring data in the trace buffer faster than they are read out.

When there are no more measuring results in the trace buffer, i.e. <BYTE 1 = 0>, 0 is output.

6.3.4 Interrogation of measuring results

Interrogation of Results after STOP (I)

Command: `RESULT? 0`

If the device is in remote control and stop status, the command `RESULT? 0` may be used to read the results of the last measurement or of a stored measurement. A binary data format is used for the results.

Data format: ARBITRARY BLOCK PROGRAM DATA (ANSI/IEEE Std 488.2)

<#> < XA> <XB1> <XB2>... <XBn> <Byte 1> ... <Byte n>

where:

<#> : Preamble

<XA> : Length of length data in bytes (in ASCII code)

<XB1>..<XBn> : Number of data bytes (in ASCII code)

<Byte 1>..<Byte n> : Measuring results of the measuring mode in question

MEASURING DATA FORMAT starting with < Byte 1>

No.	Type	Meaning
1	BYTE	Result or Trace : Trace = 0 ; Result = 1
2	BYTE	IEC address (0 - 31)
3,4	WORD	Length of header in BYTES (here 15)
5,6	WORD	Length of measurement in bytes (Structure of measuring results depends on measuring mode)
7	BYTE	not used
8	BYTE	not used
9	BYTE	not used
10	BYTE	Internal format coding, e.g. 0: Graphical results 1: Numerical results 2: ASCII string
11	BYTE	Conformance byte Evaluation whether the measuring result is within the limits of tolerance. The test required for this depends on the measuring mode (see description of measurement data structure).
12....15	BYTE	RESERVE
16....32	BYTE	17 BYTES (in ASCII code) DATE/TIME (dd:mm:yy hh:mm:ss)
33....	BYTE	Measuring results with length according to no. 5,6 ******MEASURING RESULTS******

Data types:

BYTE = 8 BITS (MSB.....LSB)

WORD = 16 BITS (LOW BYTE, HIGH BYTE)

Interrogation of Results after STOP (II)

Command: `RESULT? 1`

If the device is in remote control mode and has stopped after a measurement, the command 'RESULT? 1' can be used to output the results of the most recent measurement or of a stored measurement. Unlike the command 'RESULT? 0' an additional 300 bytes are output for the menu parameters. The data format for these parameters is in ASCII code and corresponds to that of the commands MEASURE and ART_LINE. The following data format is used for the results:

Data format: ARBITRARY BLOCK PROGRAM DATA (ANSI/IEEE Std 488.2)

<#> < XA> <XB1> <XB2>... <XBn> <Byte 1>... <Byte n>

where:

<#>	:	Preamble
<XA>	:	Length of length data in bytes (in ASCII code)
<XB1>..<XBn>	:	Number of data bytes (in ASCII code)
<Byte 1>..<Byte n>	:	Measuring results of the measuring mode in question

MEASURING DATA FORMAT starting with < Byte 1>

No.	Type	Meaning
1	BYTE	Result or Trace : Trace = 0 ; Result = 1
2	BYTE	IEC address (0 - 31)
3,4	WORD	Length of header in BYTES (here 15)
5,6	WORD	Length of measuring results in bytes (Structure of measuring results depends on measuring mode)
7	BYTE	not used
8	BYTE	not used
9	BYTE	not used
10	BYTE	Internal format coding, e.g. 0: Graphical results 1: Numerical results 2: ASCII string
11	BYTE	Conformance byte Evaluation whether the measuring result is within the limits of tolerance. The test required for this depends on the measuring mode (see description of measurement data structure).
12....15	BYTE	RESERVE
16....32	BYTE	17 BYTES (in ASCII code) DATE/TIME (dd:mm:yy hh:mm:ss)
33....232	BYTE	200 BYTES (in ASCII code) RELEVANT MEASURING MODE PARAMETERS
233....332	BYTE	100 BYTES (in ASCII code) ARTIFICIAL LINE PARAMETERS
333....	BYTE	Measuring results with length according to no. 5,6 ******MEASURING RESULTS******

Data types:

BYTE = 8 BITS (MSB.....LSB)

WORD = 16 BITS (LOW BYTE, HIGH BYTE)

Interrogation of status information during measurement

Command: `READ_STATUS?`

When the device is in remote control mode during measurement, important events which also appear as messages in the small screen window are written into an internal status buffer in the form of coded numbers. A bit is set accordingly in event register B (status available). The command `READ_STATUS?` can be entered to output the data in ASCII format:

Example:

Result after entering `READ_STATUS? --> +4, +106`

`+4` : Status buffer contains 4 status entries.

`+106` : Last status entry

If there are no more status entries, **+0** is output.

If a message is no longer relevant, the status can be canceled. The status number is then increased by 1 for the IEC user. The message window on the K1403 screen disappears at the same time.

Example: STATUS **+202** --> no INFO 1 was detected

and then

STATUS **+203** --> INFO 1 was detected (again)

Overview of status information and meanings:

Module	Status	Meaning	
ANALOG1	---------	----------	
ANALOG2	100	NO INFO1	
	102	NO TRIGGER	
	104	L1 ACTIVE	
	106	L1 NOT ACTIVE	
	108	IUT - STATE F2	
	110	IUT - STATE F3	
	112	IUT - STATE F4	
	114	IUT - STATE F5	
	116	IUT - STATE F6	
	118	IUT - STATE F7	
	120	IUT - STATE F8	
	122	IUT CONN. UPSTREAM	
	124	IUT CONN. DOWNSTREAM	
	126	WAIT 30 sec.	
Power feeding module	150	VOLTAGE SET ERROR	
	152	VOLTAGE SWITCHED OFF	
	156	INTERNAL ERROR	
	158	VOLTAGE IS INTERRUPTED	
	160	ERROR ON NT	
	162	NT-Volt. TOO LOW	
	164	NT-CUR. LIMITAT	
	166	NO VALID TRANSIENT	
	168	CALIB. ERROR 1	
	170	CALIB. ERROR 2	
	172	OVERLOAD. P>8W	
	174	NO VALID PARAMETER	
	176	SWITCH OVER, PLEASE	
	178	CALIB. ERROR NT	

Functional test	200	USER CALL	
	202	NO INFO1 DETECTED	
	204	NO INFO3 DETECTED	
	206	INFO 0 DETECTED	
	208	UNDEF. INFO DETECTED	
	210	WRONG AMPLITUDE	
	212	NO INFO 0 DETECTED	
	214	AIS (period 1)	
	216	PERMANENT ZERO (Period 0)	
	218	BITSLIP	
	220	STATE IUTCHG. -> G2	
	222	NO INFO2 DETECTED	
	224	NO INFO4 DETECTED	
	226	MEASUREMENT RESTARTED	
	228	LAYER 1 ERROR	
	230	MEASUREM. FINISHED	
	232	MEASUREM. ABORTED	
	234	NEW INTERVAL	
	236	PLL WAITING	
	238	LAYER 1 ACTIVE	
	240	LAYER 1 ACTIVE AND WAITING	
	242	NO LAYER 3 CONNECTION	
	244	LAYER 3 ESTABLISHED	
	246	WAITING FOR LOOPBACK	
Jitter option	302	NO MEASURING	
Main processor	350	READ / WRITE FAILURE (BOARDS)	
	352	EXTERNAL INVERTED VOLTAGE DETECTED	Measurement is not started due to interference voltage
	360	CALIBRATION ABORTED	Noise generator of artificial line could not be calibrated

6.4 Using the artificial line in IEC operation

The twelve parameters of the artificial line are global parameters within K1403, i.e. they are not assigned to any one measuring mode. If the artificial line option is available on the device, the user must set the parameters in the configuration desired. To ensure that the artificial line is switched off, an ART_LINE command with the parameter LINE CONFIG = 0 (OFF) should be entered. Here the possibility of interrogating with an ARTLINE command (ART_LINE?) is helpful in order to find a suitable setting without having to search through the tables of parameters.

If a measurement is to be carried out with the artificial line switched on, **first** the MEASURE **and secondly** the ART_LINE command must be entered before the START command.

If a measurement is defined without setting the artificial line, it is also not effective.

If no artificial line module is plugged into K1403, the ART_LINE command is meaningless. The measuring path without artificial line will always be chosen.

The parameter 'LINE CONFIG' is of great significance in the K1403 menu. A description of this parameter is given in the following table.

Parameter value	Effect
LINE CONFIG = 0 (OFF) **CCITT: CONFIG.4 (IDEAL)**	The artificial line module is not switched to the measuring path. *Fixed setting defined according to CCITT*
LINE CONFIG = 1 (FREELY SELECTABLE)	The following parameters are freely selectable.
LINE CONFIG = 2....5 **CCITT: CONFIG.1** **CCITT: CONFIG.2** Extended passive bus **CCITT: CONFIG.3a**	 *Fixed setting defined according to CCITT* *Fixed setting defined according to CCITT* *Fixed setting defined according to CCITT*
LINE CONFIG = 6 LC (LOW CAP. CABLE) **CCITT: CONFIG.3b**	Low capacity switching element of the artificial line is switched on. Only possible with the combined module (...A11-L160). *Fixed setting defined according to CCITT*

6.4.1 Switching off the artificial line

To switch off the artificial line, enter the complete `ART_LINE` command. The parameter 'LINE CONFIG' must be set to **0 = OFF**. The following parameters must be selected according to group and can be easily read off during configuration 'Freely selectable'. Switching the artificial line off via the IEC is only practical for the configuration of group 2.

No.	Meaning	Comments
1	LINE CONFIGURATION 0: CONFIGURATION 4 (OFF) 1: FREELY SELECTABLE 2: CONFIGURATION 1 3: CONFIGURATION 2 4: CONFIGURATION 3a 5: EXTENDED PASSIVE BUS 6: CONFIGURATION 3b	The following parameters in this table are meaningless, but have to be entered in the specified area according to group
2	K1403 ON: **0...1**	
3	LINE LENGTH: **0....5**	
4	TR NEAR: **0...1**	
5	TR REMOTE: **0...1**	
6	NOISE FREQUENCY: **0...3**	
7	NOISE DISTANCE: **0...1**	
8	NOISE TYPE: **0...1**	
9	TE NUMBER: **0...3**	
10	TE CONFIG: **0...2**	
11	RX direct **0...1**	
12	**0...1**	Parameter for service purposes

6.4.2 Parameter groups of the artificial line

Since the device may be operated either as an **isolated artificial line** or as a **measuring device with artificial line**, the following detailed parameter description has been divided into two groups (1 and 2).

Parameter values in	Characteristics
GROUP 1	**OPERATION OF THE K1403 AS AN ARTIFICIAL LINE** The parameter settings are valid for the **isolated** artificial line, i.e. the sockets at the rear of the module are effective. Thus, the module can be operated purely as an artificial line between TE and NT. To reach this mode via remote control, enter the command `MEASURE<blank> 2,0,0` Set the parameters of the artificial line via the `ART_LINE` command. In this case the setting (relay) is carried out via the command **`UPDATE<blank>99`**. ATTENTION! The RJ45 sockets at the rear of the device must be used!
GROUP 2	**OPERATION OF THE K1403 AS MEASURING DEVICE WITH ARTIFICIAL LINE** The parameter settings are valid for the following measuring modes: **Frame delay** (electrical characteristics at TE) **Receiver Input Delay** (electrical characteristics at NT) **Jitter (digital)** (electrical characteristics) **Receiver sensitivity** (electrical characteristics) **Basic interconnection** (functional tests) **Jitter (analog)** (jitter option) 1. Enter appropriate `MEASURE` command. 2. Enter appropriate `ART_LINE` command 3. Start measurement via the `START` command

6.4.3 Group 1: Freely selectable

No.	Meaning	Comments
1	LINE CONFIGURATION **1: FREELY SELECTABLE** 2: CONFIGURATION 1 3: CONFIGURATION 2 4: CONFIGURATION 3a 5: EXTENDED PASSIVE BUS 6: CONFIGURATION 3b	
2	K1403 ON: 0: Remote 1: Near	
3	LINE LENGTH: 0: 100 m ... 200 m (1 µs) 1: 500 m 2: 600 m 3: 650 m ... 750 m (6 dB) 4: 800 m 5: 1000 m	
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off 1: On	
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX 1: TX	
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs 3: 7 TEs	
10	TE CONFIG: 0: Off 1: Remote 2: Near	
11	RX direct 0: Off 1: On	
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.4 Group 1: Configuration 1

No.	Meaning	Comments
1	LINE CONFIGURATION 1: FREELY SELECTABLE **2: CONFIGURATION 1** 3: CONFIGURATION 2 4: CONFIGURATION 3a 5: EXTENDED PASSIVE BUS 6: CONFIGURATION 3b	5 fixed parameters
2	K1403 ON: **0: Remote** 1: Near	Fixed, not selectable
3	LINE LENGTH: 0: 100 m ... 200 m (1 µs) 1: 500 m 2: 600 m **3: 650 m ... 750 m (6 dB)** 4: 800 m 5: 1000 m	Fixed, not selectable
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off **1: On**	Fixed, not selectable
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX **1: TX**	Fixed, not selectable
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs 3: 7 TEs	
10	TE CONFIG: **0: Off** 1: Remote 2: Near	Fixed, not selectable
11	RX direct 0: Off 1: On	
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.5 Group 1: Configuration 2

No.	Meaning	Comments
1	LINE CONFIGURATION 1: FREELY SELECTABLE 2: CONFIGURATION 1 **3: CONFIGURATION 2** 4: CONFIGURATION 3a 5: EXTENDED PASSIVE BUS 6: CONFIGURATION 3b	6 fixed parameters
2	K1403 ON: **0: Remote** 1: Near	Fixed, not selectable
3	LINE LENGTH: **0: 100 m ... 200 m (1 µs)** 1: 500 m 2: 600 m 3: 650 m ... 750 m (6 dB) 4: 800 m 5: 1000 m	Fixed, not selectable
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off **1: On**	Fixed, not selectable
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX **1: TX**	Fixed, not selectable
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs **3: 7 TEs**	Fixed, not selectable
10	TE CONFIG: 0: Off 1: Remote **2: Near**	Fixed, not selectable
11	RX direct 0: Off 1: On	
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.6 Group 1: Configuration 3a

No.	Meaning	Comments
1	LINE CONFIGURATION 1: FREELY SELECTABLE 2: CONFIGURATION 1 3: CONFIGURATION 2 **4: CONFIGURATION 3a** 5: EXTENDED PASSIVE BUS 6: CONFIGURATION 3b	6 fixed parameters
2	K1403 ON: 0: Remote **1: Near**	Fixed, not selectable
3	LINE LENGTH: **0: 100 m ... 200 m (1 µs)** 1: 500 m 2: 600 m 3: 650 m ... 750 m (6 dB) 4: 800 m 5: 1000 m	Fixed, not selectable
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off **1: On**	Fixed, not selectable
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX **1: TX**	Fixed, not selectable
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs **3: 7 TEs**	Fixed, not selectable
10	TE CONFIG: 0: Off **1: Remote** 2: Near	Fixed, not selectable
11	RX direct 0: Off 1: On	
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.7 Group 1: Extended passive bus

No.	Meaning	Comments
1	LINE CONFIGURATION 1: FREELY SELECTABLE 2: CONFIGURATION 1 3: CONFIGURATION 2 4: CONFIGURATION 3a **5: EXTENDED PASSIVE BUS** 6: CONFIGURATION 3b	5 fixed parameters
2	K1403 ON: **0: Remote** 1: Near	Fixed, not selectable
3	LINE LENGTH: 0: 100 m ... 200 m (1 µs) **1: 500 m** 2: 600 m 3: 650 m ... 750 m (6 dB) 4: 800 m 5: 1000 m	Fixed, not selectable
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off **1: On**	Fixed, not selectable
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX **1: TX**	Fixed, not selectable
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs 3: 7 TEs	
10	TE CONFIG: 0: Off 1: Remote **2: Near**	Fixed, not selectable
11	RX direct 0: Off 1: On	
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.8 Group 1: Configuration 3b

(Only possible with artificial line models HC + LC)

No.	Meaning	Comments
1	LINE CONFIGURATION 1: FREELY SELECTABLE 2: CONFIGURATION 1 3: CONFIGURATION 2 4: CONFIGURATION 3a 5: EXTENDED PASSIVE BUS **6: CONFIGURATION 3b**	6 fixed parameters
2	K1403 ON: 0: Remote **1: Near**	Fixed, not selectable
3	LINE LENGTH: **0: 100 m ... 200 m (1 µs)** 1: 500 m 2: 600 m 3: 650 m ... 750 m (6 dB) 4: 800 m 5: 1000 m	Fixed, not selectable
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off **1: On**	Fixed, not selectable
6	NOISE FREQUENCY: 0 Off 1 200 kHz 2 2 MHz 3 External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX 1: TX	
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs **3: 7 TEs**	Fixed, not selectable
10	TE CONFIG: 0: Off **1: Remote** 2: Near	Fixed, not selectable
11	RX direct 0: Off 1: On	
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.9 Group 2: Freely selectable

No.	Meaning	Comments
1	LINE CONFIGURATION 0: CONFIGURATION 4: ideal **1: FREELY SELECTABLE** 2: CONFIGURATION 1 3: CONFIGURATION 2 4: CONFIGURATION 3a 5: *Not defined* 6: CONFIGURATION 3b	1 fixed parameter
2	K1403 ON: 0: Remote 1: Near	
3	LINE LENGTH: 0: 100 m ... 200 m (1 µs) 1: 500 m 2: 600 m 3: 650 m ... 750 m (6 dB) 4: 800 m 5: 1000 m	
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off 1: On	
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX 1: TX	
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs 3: 7 TEs	
10	TE CONFIG: 0: Off 1: Remote 2: Near	
11	RX direct 0: Off **1: On**	Fixed, not selectable
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.10 Group 2: Configuration 1

No.	Meaning	Comments
1	LINE CONFIGURATION 0: CONFIGURATION 4: ideal 1: FREELY SELECTABLE **2: CONFIGURATION 1** 3: CONFIGURATION 2 4: CONFIGURATION 3a 5: *Not defined* 6: CONFIGURATION 3b	6 fixed parameters
2	K1403 ON: **0: Remote** 1: Near	Fixed, not selectable
3	LINE LENGTH: 0: 100 m ... 200 m (1 µs) 1: 500 m 2: 600 m **3: 650 m ... 750 m (6 dB)** 4: 800 m 5: 1000 m	Fixed, not selectable
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off **1: On**	Fixed, not selectable
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX **1: TX**	Fixed, not selectable
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs 3: 7 TEs	
10	TE CONFIG: **0: Off** 1: Remote 2: Near	Fixed, not selectable
11	RX direct 0: Off **1: On**	Fixed, not selectable
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.11 Group 2: Configuration 2

No.	Meaning	Comments
1	LINE CONFIGURATION 0: CONFIGURATION 4: ideal 1: FREELY SELECTABLE 2: CONFIGURATION 1 **3: CONFIGURATION 2** 4: CONFIGURATION 3a 5: *Not defined* 6: CONFIGURATION 3b	7 fixed parameters
2	K1403 ON: **0: Remote** 1: Near	Fixed, not selectable
3	LINE LENGTH: **0: 100 m ... 200 m (1 µs)** 1: 500 m 2: 600 m 3: 650 m ... 750 m (6 dB) 4: 800 m 5: 1000 m	Fixed, not selectable
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off **1: On**	Fixed, not selectable
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX **1: TX**	Fixed, not selectable
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs **3: 7 TEs**	Fixed, not selectable
10	TE CONFIG: 0: Off 1: Remote **2: Near**	Fixed, not selectable
11	RX direct 0: Off **1: On**	Fixed, not selectable
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.12 Group 2: Configuration 3a

No.	Meaning	Comments
1	LINE CONFIGURATION 0: CONFIGURATION 4: ideal 1: FREELY SELECTABLE 2: CONFIGURATION 1 3: CONFIGURATION 2 **4: CONFIGURATION 3a** 5: *Not defined* 6: CONFIGURATION 3b	7 fixed parameters
2	K1403 ON: 0: Remote **1: Near**	Fixed, not selectable
3	LINE LENGTH: **0: 100 m ... 200 m (1 µs)** 1: 500 m 2: 600 m 3: 650 m ... 750 m (6 dB) 4: 800 m 5: 1000 m	Fixed, not selectable
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off **1: On**	Fixed, not selectable
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX **1: TX**	Fixed, not selectable
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs **3: 7 TEs**	Fixed, not selectable
10	TE CONFIG: 0: Off **1: Remote** 2: Near	Fixed, not selectable
11	RX direct 0: Off **1: On**	Fixed, not selectable
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.4.13 Group 2: Configuration 3b

No.	Meaning	Comments
1	LINE CONFIGURATION 0: CONFIGURATION 4: ideal 1: FREELY SELECTABLE 2: CONFIGURATION 1 3: CONFIGURATION 2 4: CONFIGURATION 3a 5: *Not defined* **6: CONFIGURATION 3b**	6 fixed parameters
2	K1403 ON: 0: Remote **1: Near**	Fixed, not selectable
3	LINE LENGTH: **0: 100 m ... 200 m (1 µs)** 1: 500 m 2: 600 m 3: 650 m ... 750 m (6 dB) 4: 800 m 5: 1000 m	Fixed, not selectable
4	TR NEAR: 0: Off 1: On	
5	TR REMOTE: 0: Off **1: On**	Fixed, not selectable
6	NOISE FREQUENCY: 0: Off 1: 200 kHz 2: 2 MHz 3: External	
7	NOISE DISTANCE: 0: Remote 1: Near	
8	NOISE TYPE: 0: RX **1: TX**	Fixed, not selectable
9	TE NUMBER: 0: 1 TE 1: 3 TEs 2: 5 TEs **3: 7 TEs**	Fixed, not selectable
10	TE CONFIG: 0: Off **1: Remote** 2: Near	Fixed, not selectable
11	RX direct 0: Off **1: On**	Fixed, not selectable
12	0: If par. no. 6 = 0, 3} must be 1: If par. no. 6 = 1, 2} set	Parameter for service purposes

6.5 Event and status registers

The device is equipped with special registers which can be interrogated by the user to detect operating errors (e.g. entering an incorrect command), device status (e.g. device is in status STOP) and any exceeding of limit values (e.g. exceeding tolerance limits).

Four **event** registers (**event** status register, **event** register **A, event** register **B, event** register **C**) inform the user about events which have occurred in the device since the last interrogation of the registers. For example, an incorrect command sets a fixed bit for "command error" in the event status register. This bit remains set even if the correct commands are subsequently entered. Only when the event status register is interrogated will the bit for "command error" be reset.

Each of the four event registers is assigned an enable register.

Event Status Register	ESR
Event Status Enable	ESE
Event Register A	ERA
Event Register A Enable	ERAE
Event Register B	ERB
Event Register B Enable	ERBE
Event Register C	ERC
Event Register C Enable	ERCE

A service request (SRQ) for an event which has occurred can be selectively disabled or enabled using the enable registers ESE, ERAE, ERBE and ERCE.

6.5.1 Service request

The service request (SRQ) calls on the control computer to output certain information about status or events in the device. For this purpose there is a joint line (SRQ) on the IEC bus which can be activated by any connected device.

The following command will illustrate how a service request (SRQ) takes place.

A service request (SRQ) is to be triggered by entering an incorrect command.

A precondition is that bit 5 is set in the event status enable register. The event status register should now have the value 0. When an incorrect command is received, the device sets bit 5 (command error), CME in the event status register.

As a result a logical AND operation is created between the event and the enable register which yields the value 32. Since this value does not equal 0, the sum bit (Event Summary Bit, ESB) of the event status register is set. This sum bit will be entered at the appropriate place in a status byte.

The status byte also has an enable register (Service Request Enable register, SRE). For the example described, bit 5 (enable ESB) of the SRE register must be set. The status byte and the SRE register will be ANDed and the resulting sum bit with the value 1 will be entered in the status byte itself at the position 6 (RQS). The device then triggers a service request (SRQ) via the IEC interface. Service requests from the event registers ERA, ERB and ERC are generated in the same way.

Processing a service request (SRQ)

The processing of a service request on the IEC bus will be explained with reference to the previous example.

If the SRQ line of the IEC bus switches to 'LOW', the IEC bus controller runs a "serial poll", i.e. the value of the status byte of the device requesting the SRQ is read. The RQS bit of the status byte indicates that this device has activated the SRQ. This device re-enables the SRQ line of the IEC bus by means of the "serial poll". The sum bits in the status byte can help to detect which events could have triggered the SRQ. In the present example, the sum bit EXB is set, upon which the appropriate event status register is interrogated to find out which event has occurred. The interrogation yields the value 32, which means that the bit for "command error" has been set. Interrogating the event status register will automatically erase this bit. A new sum bit is created, it receives the value 0 and is entered in the status byte. This in turn leads to the updating of the sum byte (RQS) which is also reset. If several sum bits are set in the status byte, the events can be processed consecutively in the same way.

6.5.2 Status byte (STB) with enable register (SRE)

MSB							LSB
0	RQS	ESR	MAV	ERA	ERB	ERC	0
D7	D6	D5	D4	D3	D2	D1	D0

RQS: Requested Service
ESR: Sum bit of the Event Status Register
MAV: Sum bit of the output message queue (Message Available)
ERA: Sum bit of the (device-dependent) Event Register A
ERB: Sum bit of the (device-dependent) Event Register B
ERC: Sum bit of the (device-dependent) Event Register C

Interrogating status byte: Command `*STB?` or IEC bus message sequence for "serial poll".

The status byte consists of the RQS bit (D6), the ESR sum bit (D5), the MAV bit (Message Available, D4) and the two sum bits ERA (D3), ERB (D2) and ERC (D1). The individual bits each describe the status of a register or of the output buffer.

The sum bits of the three event registers ESR, ERA, ERB and ERC have the logical value 1 if the result of their AND operation with the corresponding enable register is other than 0. In contrast, the MAV bit is set when a message is available in the output buffer of the device.

Each one of the sum bits D1-D5 can trigger an SRQ, as long as the corresponding bit is set in the enable register. If at least one bit in the status byte or in the corresponding enable register changes its value from logical 0 to logical 1, the AND operation is carried out on the two registers and an SRQ triggered if the event is not equal to 0. This means that the RQS bit is set in the status byte and the SRQ line of IEC bus is activated.

6.5.3 Service Request Enable Register (SRE)

Request: `* SRE?`

Response: >n (n = 0 and 255), decimal equivalent of the SRQ enable mask

Setting command: `* SRE n`

(n= 0 and 255), decimal equivalent of the SRQ enable mask with the following coding:

MSB							LSB
0	0	c	d	e	f	g	0
D7	D6	D5	D4	D3	D2	D1	D0

c allows SRQ in the case of event status register <> 0 and enabling by the corresponding enable bits
d allows SRQ in the case of a message (output queue not empty)
e allows SRQ in the case of device-dependent event register A <> 0 and enabling by the corresponding enable bits
f allows SRQ in the case of device-dependent event register B <> 0 and enabling by the corresponding enable bits
g allows SRQ in the case of device-dependent event register C <> 0 and enabling by the corresponding enable bits
bit=1: corresponding SRQ enabled
bit=0: corresponding SRQ disabled
x : random
Bit 6 will register 0 independently of the value set.

6.5.4 Event Status Register (ESR) with Enable Register (ESE)

Event status register

MSB							LSB
0	0	CME	EXE	0	QYE	0	OPC
D7	D6	D5	D4	D3	D2	D1	D0

CME: Command Error

Unknown command, syntax error, exceeding of the standard limit values of numerical parameters etc.

EXE: Execution Error

Exceeding of command-specific parameter limits, incompatibility of a command or parameters with the current operating status etc.

QYE: Query Error

The bit is set when the device is addressed as 'talker' and no message is ready in the output queue.

OPC: Operation Complete

Information-bit - is used, when single or multiple commands have been executed by the unit. This becomes effective only when the command *OPC has been attached to to command(s).

Request: `*ESR?`

Response: >n (n = 0 and 255), decimal equivalent of the event status register

Event status enable register

The assignment of the event status enable register is similar to that of the event status register. The bits D0, D1, D3 and D6 are irrelevant.

Request: `*ESE?`

Response: >n (n = 0 and 255), decimal equivalent of the enable mask

Setting command: `*ESE n`

(n = 0 and 255), decimal equivalent of the enable mask

6.5.5 Event Register A (ERA) with Enable Register (ERAE)

Event register A

MSB							LSB
0	0	0	d	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0

d: Trace data available

Request: `ERA?`

Response: >n (n = 0 and 255), decimal equivalent of the event register A

Event Register A Enable (ERAE)

Request: `ERAE?`

Response: >n (n = 0 and 255), decimal equivalent of the enable mask A

Setting command: `ERAE n`

(n = 0 and 255) , decimal equivalent of the enable mask A

6.5.6 Event Register B (ERB) with Enable Register (ERBE)

Event register B

MSB							LSB
0	0	0	d	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0

d: Status available

Request: `ERB?`

Response: >n (n= 0 and 255), decimal equivalent of the event register B

Event Register B Enable (ERBE)

Request: `ERBE?`

Response: >n (n = 0 and 255), decimal equivalent of the enable mask B

Setting command: `ERBE n`

(n = 0 and 255), decimal equivalent of the enable mask B

6.5.7 Parallel poll

In the event of operation with the IEC interface, the device can be interrogated with the so-called 'parallel poll'. As a response a bit is placed on a specific line of the IEC data bus. The value of this bit indicates whether one of the bits in the status byte is other than 0. However, the status byte is connected with an enable mask prior to this (PRE, Parallel Enable) by an AND operation.

MSB							LSB
0	rsv	ESR	MAV	ERA	ERB	ERC	h
D7	D6	D5	D4	D3	D2	D1	D0

rsv: sets parallel request bit, if device status is service requested
ESR: sets parallel request bit, if Event Status Register <> 0
MAV: sets parallel request bit, if output message queue not empty (Message Available)
ERA: sets parallel request bit, if Event Register A <> 0
ERB: sets parallel request bit, if Event Register B <> 0
ERC: sets parallel request bit, if Event Register C <> 0

Request: `* PRE?`

>n (n = 0 and 255), decimal equivalent of the enable mask

Setting command: `* PRE n`

(n = 0 and 255), decimal equivalent of the enable mask

The command: `*IST?`

may be scanned in the form of a message as to whether the parallel request bit has been set.

Response: 0: Parallel request bit not set

1: Parallel request bit is set

7 K1403 parameters for menu and IEC

The parameters for the K1403 menu and the control at the IEC bus are listed below.

Overview

Transmission characteristics (Group = 0)	
TE mode	NT mode
Impedance	Impedance
Unbalance	Unbalance
Pulse shape	Pulse shape
Frame delay	Transmitter output impedance active
Clock accuracy	Output peak current
Transmitter output impedance active	Jitter
Pulse balance	Receiver sensitivity
Output peak current	Receiver input delay characteristics
Jitter	
Receiver sensitivity	

Functional tests (Group = 1) (optional function)	
TE mode	NT mode
Basic interconnection test	--
Binary organization of frame	Binary organization of frame
TTCN appendix B1	
TTCN appendix B2 (optional)	

Feeder tests (Group = 2)	
TE mode	NT mode
Power consumption	Normal/restricted power output
Current/time measurement	Normal/restricted switch-on tests
Power start-up tests	Normal test type "a" NT
Switchover tests	Normal connection of 1 TE
Short interruption	Normal switch-on response
Current/transient measurement	Restricted (A) during short circuit
	Restricted (B) following short-circuit
	Restricted (C) following nominal load
	Restricted (D) following capacitive short circuit

Jitter tests (group = 3) (optional function)	
TE mode	NT mode
Jitter	Jitter

7.1 Transmission characteristics TE

7.1.1 Impedance

No.	Meaning	Comments
A	0 = TE mode	
B	0 = Electrical tests	
C	0 = Measuring mode IMPEDANCE	
1	Trans./rec. 0: Receiver 1: Transmitter	
2	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	
3	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	Only effective if par. no. 2 = normal or restricted
4	DEFAULT:0	RESERVE
5	DEFAULT:0	RESERVE
6	Frequency range 0: Edit 1: Load edit 2: 2 kHz 1 MHz 3: 2 kHz 40 kHz 4: 10 kHz 200 kHz 5: 50 kHz 1MHz	
7	Lower frequency Fmin (kHz) Range: 2.000 to 1000	Only effective if par. no.6 = edit/load edit
8	Upper frequency Fmax (kHz) Range:2.000 to 1000	Only effective if par. no.6 = edit/load edit
9	DEFAULT: 0	RESERVE
10	Transmit level_1 0: Edit 1: Load edit 2: CCITT 3: 100 mV rms 4: 200 mV rms 5: 300 mV rms 6: 400 mV rms 7: 500 mV rms	
11	Transmit level_2(mV) Range: 100....1000 mV rms	Only effective if par. no.10 = edit/load edit
12	Tol. mask 0: Off 1: On 2: On (conformance test)	

When using the IEC interface for setting the following should be considered: For frequencies of 10.0 kHz and 20.0 kHz the measurement error may be greater than 5% of the measured value due to image frequencies. The applied frequency band filter has a bandwidth of BW = 25 Hz. The measurement error which is 50 Hz higher/lower than the two above-mentioned frequencies is thus less than 5%. When measuring between 2 kHz and 1 MHz (according to CCITT) the error in the entire range is less than 5% of the measured value, since the automatically set frequencies are over 50 Hz higher/lower than the two above-mentioned frequencies.

This problem is not due for the release version C73249-A11-L80 of the ANALOG1 board.

7.1.2 Unbalance

No.	Meaning	Comments
A	0 = TE mode	
B	0 = Electrical tests	
C	1 = Measuring mode UNBALANCE	
1	DEFAULT:0	RESERVE
2	Trans./rec. 0: Receiver 1: Transmitter	
3	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	
4	DEFAULT: 0	RESERVE
5	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	Only effective if par. no. 3 = normal or restricted
6	DEFAULT:0	RESERVE
7	DEFAULT: 0	RESERVE
8	DEFAULT: 0	RESERVE
9	Frequency range 0: Edit 1: Load edit 2: 2 kHz 1 MHz 3: 80 kHz 1 MHz	
10	Lower frequency Fmin (kHz) Range: 2.000 to 1000	Only effective if par. no.9 = edit/load edit
11	Upper frequency Fmax (kHz) Range: 2.000 to 1000	Only effective if par. no.9 = edit/load edit
12	DEFAULT: 0	RESERVE
13	Transmit level_1 0: Edit 1: Load edit 2: CCITT 3: 1 V rms 4: 0.9 V rms 5: 0.8 V rms 6: 0.7 V rms	
14	Transmit level_2 Range: 100 mV rms - 1000 mV rms	Only effective if par. no.10 = edit/load edit
15	Tol. mask 0: On 1: Off 2: On (conformance test)	

When using the IEC interface for setting the following should be considered: For frequencies of 10.0 kHz and 20.0 kHz the measurement error may be greater than 5% of the measured value due to image frequencies. The applied frequency band filter has a bandwidth of BW = 25 Hz. The measurement error which is 50 Hz higher/lower than the two above-mentioned frequencies is thus less than 5%. When measuring between 2 kHz and 1 MHz (according to CCITT) the error in the entire range is less than 5% of the measured value, since the automatically set frequencies are over 50 Hz higher/lower than the two above-mentioned frequencies.

This problem is not due for the release version C73249-A11-L80 of the ANALOG1 board.

7.1.3 Pulse shape

No.	Meaning	Comments
A	0 = TE mode	
B	0 = Electrical tests	
C	2 = Measuring mode PULSE SHAPE	
1	Test pulse 0: Positive 1: Negative 2: Double pulse	
2	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	
3	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	Only effective if par. no. 2 = normal or restricted
4	Load 0: 5.6 Ω 1: 50 Ω 2: 400 Ω	
5	Tol. mask 0: Off 1: Normal (conformance test) 2: Max. Hold (conformance test) 3: Min. Hold (conformance test) 4: Average (conformance test)	
6	Filter 5MHz 0: Off 1: ON	
7	DEFAULT: 0	RESERVE
8	DEFAULT: 0	RESERVE

7.1.4 Frame delay

No.	Meaning	Comments
A	0 = TE mode	
B	0 = Electrical tests	
C	3 = Measuring mode FRAME DELAY	
1	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V-56.5 V)	Only effective if par. no. 7 = normal or restricted
2	Load 0: 50 Ω 1: 100 W	
3	DEFAULT: 0	
4	DEFAULT: 0	RESERVE
5	Clock 0: Internal 1: External (5 Hz, 0.5 UI_{pp}, Service superimp. jitter, L30) 2: External (20 Hz, 0.125 UI_{pp}, Service superimp. jitter, L30) 3: External (50 Hz, 0.05 UI_{pp}, Service superimp. jitter, L30) 4: External (2 kHz, 0.05 UI_{pp}, Service superimp. jitter, L30) 5: External, clock 12.288 Mhz	
6	Test pattern 0: BINARY '1' 1: BINARY '0' 2: 0AAH 3: 2 EXP 9 -1 4: 2 EXP 11-1 5: 2 EXP 13-1 6: 2 EXP 15-1 7: 2 EXP 17-1 8: 2 EXP 19-1	
7	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	

7.1.5 Clock accuracy

No.	Meaning	Comments
A	0 = TE mode	
B	0 = Electrical tests	
C	4 = Measuring mode CLOCK ACCURACY	
1	Gate time 0: 1 sec 1: 5 sec	
2	DEFAULT:0	RESERVE
3	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	
4	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V-56.5 V)	Only effective if par. no. 3 = normal or restricted
5	Load 0: 50 Ω 1: 100 Ω	
6	DEFAULT: 0	RESERVE
7	DEFAULT: 0	RESERVE

7.1.6 Impedance of active transmitter

No.	Meaning	Comments
A	0 = TE mode	
B	0 = Electrical tests	
C	5 = Measuring mode IMPEDANCE OF ACTIVE TRANSMITTER	
1	Test pulse 0: Positive 1: Negative 2: Double pulse	
2	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	
3	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V-56.5 V)	Only effective if par. no. 2 = normal or restricted
4	Load 0: 50 Ω 1: 400 Ω	
5	Filter 5 MHz 0: Off 1: ON	
6	DEFAULT: 0	RESERVE
7	DEFAULT: 0	RESERVE

7.1.7 Pulse unbalance

No.	Meaning	Comments
A	0 = TE mode	
B	0 = Electrical tests	
C	6 = Measuring mode PULSE UNBALANCE	
1	Unbalance 0: Area 1: Amplitude	
2	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	
3	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V-56.5 V)	Only effective if par. no. 2 = normal or restricted
4	Load 0: 50 Ω 1: 100 Ω	
5	Filter 5 MHz 0: Off 1: ON	
6	DEFAULT: 0	RESERVE
7	DEFAULT: 0	RESERVE

7.1.8 Output peak current

No.	Meaning	Comments
A	0 = TE Mode	
B	0 = Electrical tests	
C	7 = Measuring mode OUTPUT PEAK CURRENT	
1	Trans./rec. 0: Receiver 1: Transmitter	
2	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	
3	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	Only effective if par. no. 2 = normal/restricted
4	Measurement 0: Absolute 1: Relative	
5	DEFAULT: 0	Reserve
6	DEFAULT: 0	Reserve
7	DEFAULT: 0	Reserve
8	DEFAULT: 0	Reserve

The touchkey may be activated using the IEC command `UPDATE 1`.

7.1.9 Jitter

No.	Meaning	Comments
A	0 = TE mode	
B	0 = Electrical tests	
C	8 = Measuring mode JITTER	
1	DEFAULT: 0	RESERVE
2	DEFAULT: 0	RESERVE
3	Test Pattern 0: BINARY '1' 1: BINARY '0' 2: ALTERNATING PATTERN 3: 2 Exp9 -1 4: 2 Exp11 -1 5: 2 Exp13 -1 6: 2 Exp15 -1 7: 2 Exp17 -1 8: 2 Exp19 -1	
4	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10V - 56.5V)	Only effective if par. no 7 = normal/restricted
5	Load 0: 50 Ω 1: 100 Ω	
6	Clock 0: Internal 1: External	
7	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	

7.1.10 Receiver sensitivity

Only possible when the option *functional tests* is installed

No.	Meaning	Comments
A	0 = TE mode	
B	0 = Electrical tests	
C	9 = Measuring mode RECEIVER SENSITIVITY	
1	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	
2	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10V - 56.5V)	Only effective if par. no.1 = normal/restricted
3	Clock 0: Internal 1: External (5 Hz, 0.5UI_{pp}, Superimp. Jitter option) 2: External (20 Hz, 0.125ui_{pp}, Superimp. Jitter option) 3: External (50 Hz, 0.05ui_{pp}, Superimp. Jitter option) 4: External (2 kHz, 0.05ui_{pp}, Superimp. Jitter option) 5: External, clock 12.288 MHz	
4	Transmitted amplitude Range: -8 dB.....+3dB - resolution: 0.1 dB (0.....110)	
5	Data 0: Internal 1: External	
6	PRBS pattern 0: 2^9 - 1 1: 2^{11} - 1 2: 2^{15} - 1 3: 2^{20} - 1	
7	Channel selection 0: B1 + B2 1: B1 2: B2	
8	Measuring mode 0: Time measurement 1: Continuous measurement	
9	Measuring time (Edit 5sec.....300sec, resolution 1sec), (5.....300)	Only effective if par. no. 8 = time meas.
10	DEFAULT: 0	RESERVE
11	DEFAULT: 0	RESERVE

7.2 Transmission characteristics NT

7.2.1 Impedance

No.	Meaning	Comments
A	1 = NT mode	
B	0 = Electrical tests	
C	0 = Measuring mode IMPEDANCE	
1	Trans./rec. 0: Receiver 1: Transmitter	
2	DEFAULT: 0	RESERVE
3	DEFAULT: 0	RESERVE
4	DEFAULT: 0	RESERVE
5	DEFAULT: 0	RESERVE
6	Frequency range 0: Edit 1: Load edit 2: 2 kHz 1 MHz 3: 2 kHz 40 kHz 4: 10 kHz 200 kHz 5: 50 kHz 1MHz	
7	Lower frequency Fmin (kHz) Range: 2.000 to 1000	Only effective if par. no. 6 = edit/load edit
8	Upper frequency Fmax (kHz) Range: 2.000 to 1000	Only effective if par. no. 6 = edit/load edit
9	DEFAULT: 0	RESERVE
10	Transmit level_1 0: Edit 1: Load edit 2: CCITT 3: 100 mV rms 4: 200 mV rms 5: 300 mV rms 6: 400 mV rms 7: 500 mV rms	
11	Transmit level_2 Range: 100 mV rms -500 mV rms	Only effective if par. no. 10 = edit/load edit
12	Tol. mask 0: Off 1: On 2: On (conformance test)	

When using the IEC interface for setting the following should be considered: For frequencies of 10.0 kHz and 20.0 kHz the measurement error may be greater than 5% of the measured value due to image frequencies. The applied frequency band filter has a bandwidth of BW = 25 Hz. The measurement error which is 50 Hz higher/lower than the two above-mentioned frequencies is thus less than 5%. When measuring between 2 kHz and 1 MHz (according to CCITT) the error in the entire range is less than 5% of the measured value, since the automatically set frequencies are over 50 Hz higher/lower than the two above-mentioned frequencies.

This problem is not due for the release version C73249-A11-L80 of the ANALOG1 board.

7.2.2 Unbalance

No.	Meaning	Comments
A	1 = NT mode	
B	0 = Electrical tests	
C	1 = Measuring mode UNBALANCE	
1	DEFAULT: 0	RESERVE
2	Trans./rec. 0: Receiver 1: Transmitter	
3	DEFAULT: 0	RESERVE
4	DEFAULT: 0	RESERVE
5	DEFAULT: 0	RESERVE
6	DEFAULT: 0	RESERVE
7	Frequency range 0: Edit 1: Load edit 2: 2 kHz 1 MHz 3: 80 kHz 1 MHz	
8	Lower frequency Fmin (kHz) Range: 2.000 to 1000	Only effective if par. no. 7 = edit/load edit
9	Upper frequency Fmax (kHz) Range: 2.000 to 1000	Only effective if par. no. 7 = edit/load edit
10	DEFAULT: 0	RESERVE
11	Transmit level_1 0: Edit 1: Load edit 2: CCITT 3: 1 V rms 4: 0.9 V rms 5: 0.8 V rms 6: 0.7 V rms	
12	Transmit level_2 Range: 700 mV rms - 1 V rms	Only effective if par. no. 11 = edit/load edit
13	Tol. mask 0: Off 1: On 2: On (conformance test)	

When using the IEC interface for setting the following should be considered: For frequencies of 10.0 kHz and 20.0 kHz the measurement error may be greater than 5% of the measured value due to image frequencies. The applied frequency band filter has a bandwidth of BW = 25 Hz. The measurement error which is 50 Hz higher/lower than the two above-mentioned frequencies is thus less than 5%. When measuring between 2 kHz and 1 MHz (according to CCITT) the error in the entire range is less than 5% of the measured value, since the automatically set frequencies are over 50 Hz higher/lower than the two above-mentioned frequencies.

This problem is not due for the release version C73249-A11-L80 of the ANALOG1 board.

7.2.3 Pulse shape

No.	Meaning	Comments
A	1 = NT mode	
B	0 = Electrical tests	
C	2 = Measuring mode PULSE SHAPE	
1	Test pulse 0: Positive 1: Negative	
2	DEFAULT: 0	RESERVE
3	Tol. mask 0: Off 1: Normal (conformance test) 2: Max. Hold (conformance test) 3: Min. values (conformance test) 4: Average (conformance test)	
4	Filter 5 MHz 0: Off 1: On	
5	DEFAULT: 0	RESERVE
6	DEFAULT: 0	RESERVE

7.2.4 Impedance of active transmitter

No.	Meaning	Comments
A	1 = NT mode	
B	0 = Electrical tests	
C	3 = Measuring mode IMPEDANCE OF ACTIVE TRANSMITTER	
1	Test pulse 0: Positive 1: Negative	
2	DEFAULT: 0	RESERVE
3	Filter 5 MHz 0: Off 1: On	
4	DEFAULT: 0	RESERVE
5	DEFAULT: 0	RESERVE

7.2.5 Output peak current

No.	Meaning	Comments
A	1 = NT mode	
B	0 = Electrical tests	
C	4 = Measuring mode OUTPUT PEAK CURRENT	
1	Trans./rec. 0: Receiver 1: Transmitter	
2	Measuring 0: Absolute 1: Relative	
3	DEFAULT: 0	RESERVE
4	DEFAULT: 0	RESERVE
5	DEFAULT: 0	RESERVE

The touchkey can be activated using the IEC command `UPDATE 1`.

7.2.6 Jitter

No.	Meaning	Comments
A	1 = NT mode	
B	0 = Electrical tests	
C	5 = Measuring mode JITTER	
1	DEFAULT: 0	RESERVE
2	Test pattern 0: B1=B2=D=E=1 (binary '1') 1: B1=B2=D=E=0 (binary '0') 2: Alternating pattern: AAH / 0 3: 2 EXP 9-1 4: 2 EXP 11-1 5: 2 EXP 13-1 6: 2 EXP 15-1 7: 2 EXP 17-1 8: 2 EXP 19-1	
3	Load 0: 50 Ω 1: 100 Ω	
4	DEFAULT: 0	RESERVE
5	DEFAULT: 0	RESERVE
6	DEFAULT: 0	RESERVE

7.2.7 Receiver sensitivity

Only available with the *functional tests* option.

No.	Meaning	Comments
A	1 = NT mode	
B	0 = Electrical tests	
C	6 = Measuring mode RECEIVER SENSITIVITY	
1	DEFAULT: 0	RESERVE
2	DEFAULT: 0	RESERVE
3	Clock 0: Internal 1: External (5 Hz, 0.5UI_{pp}, superimp. Jitter option) 2: External (20 Hz, 0.125UI_{pp}, superimp. Jitter option) 3: External (50 Hz, 0.05UI_{pp}, superimp. Jitter option) 4: External (2 kHz, 0.05UI_{pp}, superimp. Jitter option) 5: External, clock 12.288 MHz	
4	Transmit. amplitude Range: -8 dB.....+3dB - Resolution: 0.1 dB (0.....110)	
5	Data 0: Internal 1: External	
6	PRSB pattern 0: $2^9 - 1$ 1: $2^{11} - 1$ 2: $2^{15} - 1$ 3: $2^{20} - 1$	
7	Channel selection 0: B1 + B2 1: B1 2: B2	
8	Measuring mode 0: Time measurement 1: Continuous measurement	
9	Measuring time (Edit 5sec.....300sec, resolution 1sec) (5.....300)	Only effective if par.no.8=time measurement

7.2.8 Receiver input delay characteristics

Only available with the *functional tests* option.

No.	Meaning	Comments
A	1 = NT mode	
B	0 = Electrical tests	
C	7 = Measuring mode RECEIVER INPUT DELAY CHARACT.	
1	DEFAULT: 0	RESERVE
2	DEFAULT: 0	RESERVE
3	Frame delay + 2UI Range: -8 µs....+35µs (resolution: 1 µs) (0.....43)	
4	Transmit. amplitude Range: -8 dB.....+3dB - resolution: 0.1 dB (0.....110)	
5	Data 0: Internal 1: External	
6	PRBS pattern 0: $2^9 - 1$ 1: $2^{11} - 1$ 2: $2^{15} - 1$ 3: $2^{20} - 1$	
7	Channel selection 0: B1 + B2 1: B1 2: B2	
8	DEFAULT: 0	RESERVE
9	Measuring time (Edit 5sec.....300sec, resolution 1 sec) (5.....300)	Only effective if par. no. 8 = time measurement

7.3 Functional tests TE

7.3.1 Basic Interconnection test

Only available with the *functional tests* option.

No.	Meaning	Comments
A	0 = TE mode	
B	1 = Functional Tests	
C	0 = Measuring mode BASIC INTERCONNECTION TEST	
1	Aktivierung 0: Activation active 1: Activation passive 2: Basic interconnection test upstream 3: Basic interconnection test downstream	DEFAULT: 0
2	Power feeding 0: Passive 1: Normal 2: RESTRICTED 3: External	
3	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	Only effective if par. no. 2 = normal or restricted
4	Data link 0: Internal 1: External	
5	PRBS_PATTERN 0: 2 EXP 9 -1 1: 2 EXP 11-1 2: 2 EXP 15-1 3: 2 EXP 20-1	
6	Channels 0: B1 + B2 1: B1 2: B2	Not possible if par. no. 1 = active or passive
7	Measuring time in seconds from 1 s...300 s Measuring time=0: continuous measurement Range: 0 - 300	DEFAULT: 60 s
8	Information transmission capability (SETUP parameters) 0: Speech 1: Audio 3.1 kHz 2: Data 3: Audio 7.0 kHz 4: Video 5: User-defined (not used)	Only effective if par. no. 1 ={2,3}
9	DEFAULT: 0	RESERVE
10	DEFAULT: 0	RESERVE

7.3.2 Binary organisation of frame

Only available with the *functional tests* option.

No.	Meaning	Comments
A	0 = TE mode	
B	1 = Functional Tests	
C	1 = Measuring mode BINARY ORGANISATION OF FRAME	
1	Test 0: Info 3 1: Info 1	DEFAULT: 0
2	Power feeding 1: Normal 2: RESTRICTED 3: External	
3	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	Only effective if par. no. 2 = normal or restricted
4	PRBS_PATTERN 0: 2 EXP 9 -1 1: 2 EXP 11-1 2: 2 EXP 15-1 3: 2 EXP 20-1	Only effective if par. no. 1 = info 3 (0)
5	Channels 0: B1 + B2 1: B1 2: B2 3: B1 + B2 + D	
6	DEFAULT: 0	RESERVE
7	DEFAULT: 0	RESERVE
8	DEFAULT: 0	RESERVE

7.3.3 TTCN tests APPENDIX B1/B2

TTCN Tests APPENDIX B1

Only available with the *functional tests* option.

No.	Meaning	Comments
A	0 = TE mode	
B	1 = Functional Tests	
C	2 = Measuring mode TTCN TESTS (APP-B1)	
1	Test mode 0: D channel access control 1: Activation/deactivation 2: Timer tests 3: Frame loss 4: Multiframing 5: Idle channel code	
2	Test number (selectable via cursor) 0.. 11 for test mode = 0 0.. 57 for test mode = 1 0.. 12 for test mode = 2 0.. 6 for test mode = 3 0 for test mode = 4 0 for test mode = 5	Depends on parameter 1 and on the test suite parameters. The dependency of the test number on the test suite parameters can be found in **CTS-2-ISDN Basic Access**
3	Information transmission capability 0: Speech 1: Audio 3.1 kHz 2: Data 3: Audio 7.0 kHz 4: Video	
4	Power feeding 1: Normal 2: RESTRICTED 3: External	
5	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	Only effective if par. no. 2 = normal or restricted
6	Timer TWAIT in increments of 1s Range: 0-250s	
7	TEI_ASSIGN 0: Off 1: On	Must equal 1 if par. no. 18 = 0
	TEST SUITE PARAMETERS	
8	PC_PS 0: TE is not fed via power source 1: TE is fed via power source	
9	PC_DE 0: Power source is not detectable 1: Power source is detectable	Only effective if par. no. 8 = 0

10	PC_T309 0: Timer T309 is not available 1: Timer T309 is available	
11	PX_PR_CLASS 0: Priority class 1 1: Priority class 2	
12	PX_T3 Op. time of Timer 3 in ms (1000.....50000)	
13	PC_TEI-CONNECT 0: No 1: Yes	Only effective if par. no. 18 = 0
14	Self-test time of TE in s (0....4400)	
15	DEFAULT: 0	RESERVE
16	PX_N_FRAMES (number of possible bad frames (2...250))	
17	PX_M_FRAMES (number of necessary good frames (3...250))	
18	PC_AUTOMAT_TEI 0: No 1: Yes	
19	PC_T303 0: No 1: Yes	Only effective in APPENDIX B2 *)
20	PX_T309 (Timer operating time T309 in s (0...1000))	Only effective in APPENDIX B2 *)
21	PX_T_Appl1 (Timer operating time in s (0.....600)), resolution in 10 ms	Only effective in APPENDIX B2 *)
22	PX_T_Appl2 (Timer operating time in s (0.....600)), resolution in 10 ms	Only effective in APPENDIX B2 *)

A TTCN test is started with the command `UPDATE 1`.

`UPDATE 2` stops a test which is already running.

*) Parameters must be set within their valid limits!

TTCN tests APPENDIX B2

Only available with the *functional tests* option + *OPTION APP B2.*

No.	Meaning	Comments
A	0 = TE mode	
B	1 = Functional tests	
C	3 = Measuring mode TTCN TESTS (APP-B2)	
1	Test mode 0: D-channel access control 1: Activation/deactivation	
2	Test number 0.. 3 for test mode = 0 0.. 43 for test mode =1	Depends on parameter 1 and on the test suite parameters. The dependency of the test number on the test suite parameters can be found in **CTS-2-ISDN Basic Access**
3	Information transmission capability 0: Speech 1: Audio 3.1 kHz 2: Data 3: Audio 7.0 kHz 4: Video	
4	Power feeding 1: Normal 2: RESTRICTED 3: External	
5	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	Only effective if par. no. 2 = normal or restricted
6	Timer TWAIT in increments of 1 s Range: 0-250 s	
7	TEI_ASSIGN 0: Off 1: On	Must equal 1 if par. no. 18 = 0
	TEST SUITE PARAMETERS	
8	PC_PS 0: TE is not fed via power source 1: TE is fed via power source	
9	PC_DE 0: Power source is not detectable 1: Power source is detectable	Only effective if par no. 8 =0
10	PC_T309 0: Timer T309 is not available 1: Timer T309 is available	

11	PX_PR_CLASS 0: Priority class 1 1: Priority class 2	
12	PX_T3 Timer 3 operating time in ms (1000.....50000)	
13	PC_TEI-CONNECT 0: No 1: Yes	Only effective if par no. 18 = 0
14	Self-test time of TE in s (0....4400)	
15	DEFAULT: 0	RESERVE
16	PX_N_FRAMES (number of possible bad frames (2...250))	
17	PX_M_FRAMES (number of necessary good frames (3...250))	
18	PC_AUTOMAT_TEI 0: No 1: Yes	
19	PC_T303 0: No 1: Yes	
20	PX_T309 (Timer operating time T309 in s (0...1000))	
21	PX_T_Appl1 (Timer operating time in s (0.....600)), resolution in 10ms	
22	PX_T_Appl2 (Timer operating time in s (0.....600)), resolution in 10ms	

A TTCN test is started with the command `UPDATE 1`.

`UPDATE 2` stops a test which is already running.

7.4 Functional tests NT

7.4.1 Binary organization of frame

Only available with the *functional tests* option.

No.	Meaning	Comments
A	1 = NT mode	
B	1 = Functional tests	
C	1 = Measuring mode BINARY ORGANIZATION OF FRAME	
1	Test type 0: Info 4 1: Info 2	
2	DEFAULT: 0	RESERVE
3	DEFAULT: 0	RESERVE
4	PRBS_PATTERN 0: 2 EXP 9 -1 1: 2 EXP 11-1 2: 2 EXP 15-1 3: 2 EXP 20-1	Only effective if par. no. 1 = info 4 (0)
5	Channels 0: B1 + B2 1: B1 2: B2 3: B1 + B2 + D	Only effective if par. no. 1 = info 4 (0)

7.5 Power feeding tests TE

7.5.1 Power consumption

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	0 = Measuring mode POWER CONSUMPTION	
1	State 0: Not activated 1: Measurement before Fx 2. Measurement after Fx	
2	Power feeding 0: Normal PS1 1: Restricted PS1 2: Normal PS2 3: Restricted PS2	
3	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	
4	Serial resistance in steps of 0.1 Ω Range: 0-1280 (0 - 128)	
5	Range select 0: 0..230 mA 1: 0..38 mA 2: 0..6 mA 3: 0..750 uA 4: 0..90 uA	
6	Measure after activation, in steps of 100 ms	Only effective if par. no. 1 = {2}
7	Measure after switching on, in steps of 100 ms	Only effective if par. no. 1 = {0,1}
8	Status FX 0: F2 1: F3 2: F4 3: F5 4: F6 5: F7 6: F8 7: Basic interconnection upstream 8: Basic interconnection downstream	Only effective if par. no. 1 = {1,2}
9	S0-R 0: 50 Ω 1: 100 Ω	
10	Channels 0: B1 1: B2	Only effective if par. no. 1 = {1, 2} and par. no. 8 = {7, 8}

11	Information transmission capability (SETUP-parameters) 0: Speech 1: Audio 3,1 kHz 2: Data 3: Audio 7,0 kHz 4: Video 5: user defined (not used)	Only effective if par. no. 1 = {2,3} par. no. 8 = {7, 8}
12	Default 0	Reserve
13	Default 0	Reserve

The touchkey 'New min./max. values' may be activated by using the IEC command `UPDATE 1`.

7.5.2 Current/time measurements

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	1= Measuring mode CURRENT/TIME	
1	Power feeding 0: Normal 1: Restricted	
2	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	
3	Sampling 0: Slow 1: Fast	
4	Range select 1 0: 0..230 mA 1: 0..70 mA 2: 0..38 mA 3: 0.. 6 mA 4: 0..750 uA 5: 0..90 uA Range select 2 0: 0..250 mA 1: 0.. 70 mA 2: 0.. 23 mA 3: 0..5.5 mA 4: 0..350 µA	Range select 1, if par. no. 3 = 0 Range select 2, if par. no. 3 = 1
5	Meas. time 0: 1 s 1: 2 s 2: 4 s 3: 8 s 4: 25 ms 5: 125 ms 6: 250 ms 7: 500 ms Sampling rate 0: 10 MHz 1: 5 MHz 2: 2 MHz 3: 1 MHz 4: 0.5 MHz	Measuring time, if par. no. 3 = 0 Sampling rate , if par. no. 3 = 1
6	DEFAULT: 0	RESERVE

7.5.3 Power start-up tests

Overview

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	2 = Measuring mode POWER START-UP TESTS	
1	Power start-up mode 0: Following short-circuit 1: At low input voltage	
2	Power feeding 0: Normal 1: Restricted	
3	Power feeding voltage in steps of 1/4 volt Range: 96 -226 (24 V - 56.5 V)	Only effective if par. no. 1 = 0
4	S0-R 0: 50 Ω 1: 100 Ω	
5	Source type 0: ETS network 1: Current limitation	Only effective if par. no. 1 = 0
6	Rise time 0-24 V in steps of 1ms from 100 ms....10 s	Only effective if par. no. 1 and par. no. 5 = 0
7	Rise time 24 V-V_{End} in steps of 1 ms from 100 ms....10 s	Only effective if par. no. 1 and par. no. 5 = 0
8	Voltage on test end in steps of 0.25 V from 24 V.....56.5 V	Only effective if par. no. 1 and par. no. 5 = 0
9	Current in steps of 1 mA from 1 mA.....150 mA	Only effective if par. no. 1 = 0 and par. no. 5 = 1
10	Test mode 2: Test mode A 3: Test mode B	
11	DEFAULT: 0	RESERVE

Power start-up test (1)

Start-up mode: following short-circuit; power feeding normal; source type: ETS network

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	2 = Measuring mode POWER START-UP TESTS	
1	Start-up mode **0: Following short-circuit** 1: At low input voltage	
2	Power feeding 0: Normal **1: Restricted**	
3	Power feeding voltage in steps of 1/4 volt Range: 96 -226 (24 V - 56.5 V)	Not effective*)
4	S0-R 0: 50 Ω 1: 100 Ω	
5	Source type **0: ETS network** 1: Current limitation	
6	Rise time 0-24 V Must be **133**, if par.10 = 2 Must be **233**, if par.10 = 3	
7	Rise time 24 V-V_{End} Must be **3200**, if par. 10 = 2 Must be **5600**, if par. 10 = 3	
8	End voltage in steps of 0.25 V from 24 V.....56.5 V	
9	Current in steps of 1 mA from 1 mA.....150 mA	Not effective*)
10	Test mode 2: Test mode A 3: Test mode B	
11	DEFAULT: 0	RESERVE

*) Parameters must be set within their limits.

Power start-up test (2)

Start-up mode: following short-circuit; power feeding restricted; source type: ETS network

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	2 = Measuring mode POWER START-UP TESTS	
1	Start-up mode **0: Following short-circuit** 1: At low input voltage	
2	Power feeding 0: Normal **1: Restricted**	
3	Power feeding voltage in steps of 1/4 volt Range: 96 -226 (24 V - 56.5 V)	Not effective*)
4	S0-R 0: 50 Ω 1: 100 Ω	
5	Source type **0: ETS network** 1: Current limitation	
6	Rise time 0-24 V Must be **873** if par. 10 = 3	
7	Rise time 24 V-V_{End} Must be **4270** if par. 10 = 3	
8	End voltage in steps of 0.25 V from 24 V.....56.5 V	
9	Current in steps of 1 mA from 1 mA.....150 mA	Not effective*)
10	Test mode Must be **test mode B** (= 3)	
11	DEFAULT: 0	RESERVE

*) Parameters must be set within their limits.

Power start-up test (3)

Start-up mode: following short circuit; source type: current limitation

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	2 = Measuring mode POWER START-UP TESTS	
1	Start-up mode **0: Following short circuit** 1: At low input voltage	
2	Power feeding 0: Normal 1: Restricted	
3	Power feeding voltage in steps of 1/4 volt Range: 96 -226 (24 V - 56.5 V)	Not effective*)
4	S0-R 0: 50 Ω 1: 100 Ω	
5	Source type 0: ETS network **1: Current limitation**	
6	Rise time 0-24 V in steps of 1 ms from 100 ms....10 s	Not effective*)
7	Rise time 24 V-V_{End} in steps of 1 ms from 100 ms....10 s	Not effective*)
8	End voltage in steps of 0.25 V from 24 V.....56.5 V	
9	Current in steps of 1 mA from 1 mA.....150 mA	
10	Test mode 2: Test mode A 3: Test mode B	Not effective*)
11	DEFAULT: 0	RESERVE

*) Parameters must be set within their limits.

Power start-up test (4)

Start-up mode: at low voltage

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	2 = Measuring mode POWER START-UP TESTS	
1	Start-up mode 0: Following short-circuit **1: At low input voltage**	
2	Power feeding 0: Normal 1: Restricted	Not effective*)
3	Power feeding voltage in steps of 1/4 volt Range: 96 -226 (24 V - 56.5 V)	
4	S0-R 0: 50 Ω 1: 100 Ω	
5	Source type 0: ETS network 1: Current limitation	Not effective*)
6	Rise time 0-24 V in steps of 1 ms from 100ms....10s	Not effective*)
7	Rise time 24 V V_{End} in steps of 1 ms from 100 ms....10 s	Not effective*)
8	End voltage in steps of 0.25 V from 24 V.....56.5 V	Not effective*)
9	Current in steps of 1 mA from 1 mA.....150 mA	Not effective*)
10	Test mode 2: Test mode A 3: Test mode B	Not effective*)
11	DEFAULT: 0	RESERVE

*) Parameters must be set within their limits.

7.5.4 Switchover tests

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	3= Measuring mode SWITCHOVER TESTS	
1	Mode 0: Normal after restricted 1: Restricted after normal	
2	Normal feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	
3	Restricted feeding voltage in steps of 1/4 volt. Range: 40-226 (10 V - 56.5 V)	
4	S0-R 0: 50 Ω 1: 100 Ω	
5	Switchover time in steps of 1 ms Range: 5 ms - 250 ms	Only effective if par. no. 1 = 0
6	Range select 0: 0..230 mA 1: 0.. 70 mA 2: 0.. 38 mA 3: 0.. 6 mA 4: 0.. 750 uA 5: 0.. 90 uA	Only effective if par. no. 1 = 1
7	Current limitation in 1 mA steps of 1mA.....30mA	Only effective if par. no. 1= 0
8	Channels 0: B1 1: B2	Only effective if par. no. 1 = {1, 2} and par. no. 8 = {7, 8}
9	Information transmission capability (SETUP-parameters) 0: Speech 1: Audio 3,1 kHz 2: Data 3: Audio 7,0 kHz 4: Video 5: user defined (not used)	Only effective if par. no. 1 = 1 und par. no. 10 = 1, 2
10	Control 0: external voltage dips manual 1: internal voltage dips manual 2: internal voltage dips automatical	only permitted, if par. no. 1 = 0
11	DEFAULT: 0	RESERVE

The touchkey 'Switchover' may be activated using the IEC command `UPDATE 1`.

7.5.5 Short interruption

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	4 = Measuring mode SHORT INTERRUPTION	
1	Type of interruption 0: At TE with detector 1: Voltage interruption on TE	
2	Power feeding 0: Normal 1: Restricted	
3	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	
4	S0-R 0: 50 Ω 1: 100 Ω	
5	Interruption time Range: 1 ms ...5000 ms	
6	Status FX 0: F4 1: F6 2: F7	Only effective if par. no. 1= 0
7	DEFAULT: 0	RESERVE
8	Channels 0: B1 1: B2	Only effective if par. no. 1 = 1 und par. no. 10 = 1, 2
9	Information transmission capability (SETUP-parameters) 0: Speech 1: Audio 3,1 kHz 2: Data 3: Audio 7,0 kHz 4: Video 5: user defined (not used)	Only effective if par. no. 1 = 1 und par. no. 10 = 1, 2
10	Control 0: external voltage dips manual 1: internal voltage dips manual 2: internal voltage dips automatical	only permitted, if par. no. 1 = 0
11	Basic interconnection **0: upstream** 1: downstream	

The touchkey 'Interrupt voltage' may be activated using the IEC command `UPDATE 1`.

7.5.6 Current/transients

No.	Meaning	Comments
A	0 = TE mode	
B	2 = Power feeding tests	
C	5 = Measuring mode CURRENT/TRANSIENTS TE	
1	Power feeding 0: Normal 1: Restricted	
2	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	
3	Status FX 0: F3 1: F4 2: F5 3: F6 4: F7 5: F8 6: Basic interconnection upstream 7: Basic interconnection downstream	
4	Range select 0: 0... 70 mA 1: 0 .. 23 mA	
5	Sampling rate 0: 5 MHz 1: 10 MHz	
6	Signal source 0: Internal 1: External 0... 0.4V	
7	Trigger slope 0: Positive 1: Negative	
8	Trigger gradient 0: 3.0 mA/us 1: 3.5 mA/us 2: 4.0 mA/us 3: 4.5 mA/us 4: 5.0 mA/us 5: 5.5 mA/us 6: 6.0 mA/us 7: 6.5 mA/us 8: 7.0 mA/us	
9	Channels 0: B1 1: B2	Only effective if par. no. 3= 6, 7

10	Information transmission capability (SETUP-parameters) 0: Speech 1: Audio 3,1 kHz 2: Data 3: Audio 7,0 kHz 4: Video 5: user defined (not used)	Only effective if par. no. 3 = 6, 7
11	DEFAULT: 0	RESERVE
12	DEFAULT: 0	RESERVE
13	DEFAULT: 0	RESERVE

7.6 Power feeding tests NT

The measuring modes switch-on/switchover tests, overload tests, load change tests of the power feeding conditions on NT are only available as of software version V4.0.

7.6.1 Normal/restricted power output

No.	Meaning	Comments
A	1 = TE mode	
B	2 = Power feeding tests	
C	0 = Measuring mode normal/restricted POWER OUTPUT NT	
1	Power feeding 0: PS1 1: PS2	
2	Minimum voltage (PS1) in steps of 1 V Range: 1-56 (1V - 56V)	Only effective if par. no. 1 = 0
3	Minimum voltage (PS2) in steps of 1 V Range: 1-56 (1 V - 56 V)	Only effective if par. no. 1 = 1
4	Maximum load current in steps of 0.25 mA Range: 0-1200 (0 - 300 mA)	
5	Minimum load current in steps of 0.25 mA Range: 0-1200 (0 - 300 mA)	
6	Current change delta I in steps of 0.25 mA Range: 0-80 (0 - 20 mA)	
7	Duration of delta I in steps of 0.1 s Range: 1-100 (0.1 - 10 s)	
8	S0-R 0: 50 Ω 1: 100 Ω	
9	Averaging time 0: 50 ms 1: 100 ms	
10	Interface (for optional control of external loads) Range: 0-15 (0 - 15)	
11	DEFAULT: 0	RESERVE
12	DEFAULT: 0	RESERVE

7.6.2 Normal/restricted: switchover tests

Command: `MEASURE [A],[B],[C]>[1],[2],...,[9]`

No.	Meaning	Comments
A	1 = Measurements on the NT	
B	2 = Power feeding tests	
C	1 = Measuring mode NORMAL/RESTRICTED: SWITCHOVER TESTS	
1	Switchover 0: Normal ---> restricted 1: Restricted ---> normal	0: Default
2	Load 0: Internal 1: External	0: Default
3	Load current normal (in steps of 1 mA) Range: 1..300 (1...300 mA)	100: Default
4	Default 0	Reserve
5	S0 - R 0: 50 Ω 1: 100 Ω	1: Default
6	Default 0	Reserve
7	Interface 1..15	0: Default
8	Default 0	Reserve
9	Default 0	Reserve

7.6.3 Normal: test type „a“ NTs

Command: `MEASURE [A],[B],[C]>[1],[2],...,[8]`

No.	Meaning	Comments
A	1 = Measurements on the NT	
B	2 = Power feeding tests	
C	2 = Measuring mode NORMAL: TEST TYPE „a“ NTs	
1	Load 0: Internal 1: External	0: Default
2	Load curent (in steps of 1 mA) Range: 1..300 (1...300 mA)	60: Default
3	Load capacity (in steps of 10 µF) Range: 5....100 (50...1000 µF)	40: Default
4	Short-circuit time (in steps of 1 s) Range: 1...3600 (1..3600 s)	1800: Default [30min]
5	S0 - R 0: 50 Ω 1: 100 Ω	1: Default
6	Interface 1..15	0: Default
7	Default 0	Reserve
8	Default 0	Reserve

7.6.4 Normal: connection of 1 TE

Command: `MEASURE [A],[B],[C]>[1],[2],...,[6]`

No.	Meaning	Comments
A	1 = Measurements on the NT	
B	2 = Power feeding tests	
C	3 = Measuring mode NORMAL: CONNECTION OF 1 TE	
1	Load current at start (in steps of 1 mA) Range: 1..300 (1....300 mA)	90: Default
2	Averaging time 0: 50 ms 1: 100 ms	1: Default
3	S0 - R 0: 50 Ω 1: 100 Ω	1: Default
4	Interface 1..15	0: Default
5	Default 0	0: Reserve
6	Default 0	0: Reserve

7.6.5 Normal: Switch-on response

Command: `MEASURE [A],[B],[C]>[1],[2],...,[7]`

No.	Meaning	Comments
A	1 = Measurements at NT	
B	2 = Power feeding tests	
C	4 = Measuring mode NORMAL: SWITCH-ON RESPONSE	
1	Load current (T < 100 ms), (in steps of 1mA) Range: 1..360 (1....360 mA)	180: Default (4 TEs)
2	Load current (T > 100 ms), (in steps of 1 mA) Range: 1..300 (1....300 mA)	100: Default (4 TEs)
3	S0 - R 0: 50 Ω 1: 100 Ω	1: Default
4	Averaging time 0: 50 ms 1: 100 ms	0: Default
5	Interface 1..15	0: Default
6	Default 0	0: Reserve
7	Default 0	0: Reserve

7.6.6 Restricted (A): during short circuit

Command: `MEASURE [A],[B],[C]>[1],[2],...,[5]`

No.	Meaning	Comments
A	1 = Measurements on NT	
B	2 = Power feeding tests	
C	5 = Measuring mode RESTRICTED (A): AT SHORT CIRCUIT	
1	S0 - R 0: 50 Ω 1: 100 Ω	1: Default
2	Averaging time 0: 50 ms 1: 100 ms	0: Default
3	Interface 1..15	0: Default
4	Default 0	0: Reserve
5	Default 0	0: Reserve

7.6.7 Restricted (B): following short circuit

Command: `MEASURE [A],[B],[C]>[1],[2],...,[6]`

No.	Meaning	Comments
A	1 = Measurements on NT	
B	2 = Power feeding tests	
C	6 = Measuring mode RESTRICTED (B): FOLLOWING SHORT CIRCUIT	
1	1 V step duration (in steps of 100 ms) Range: 2....100 (0.2.....10 s)	2: Default
2	S0 - R 0: 50 Ω 1: 100 Ω	1: Default
3	Averaging time 0: 50 ms 1: 100 ms	0: Default
4	Interface 1..15	0: Default
5	Default 0	0: Reserve
6	Default 0	0: Reserve

7.6.8 Restricted (C): following nominal load

Command: `MEASURE [A],[B],[C]>[1],[2],...,[7]`

No.	Meaning	Comments
A	1 = Measurements on NT	
B	2 = Power feeding tests	
C	7 = Measuring mode RESTRICTED (C): FOLLOWING NOMINAL LOAD	
1	Averaging time 0: 50 ms 1: 100 ms	0: Default
2	Load current at start (in steps of 500 µA) Range: 1...21 (0.5....10.5 mA)	21: Default
3	Duration of ΔI (in steps of 100 ms) Range: 2....100 (0.2.....10 s)	2: Default
2	S0 - R 0: 50 Ω 1: 100 Ω	1: Default
4	Interface 1..15	0: Default
6	Default 0	0: Reserve
7	Default 0	0: Reserve

7.6.9 Restricted (D): following capacitive short circuit

Command: `MEASURE [A],[B],[C]>[1],[2],...,[7]`

No.	Meaning	Comments
A	1 = Measurements on NT	
B	2 = Power feeding tests	
C	8 = Measuring mode RESTRICTED (D): FOLLOWING CAP. SHORT CIRCUIT	
1	Load 0: INTERNAL 1: EXTERNAL	0: Default
2	Load capacity (in steps of 10 µF) Range: 5....100 (50...1000 µF)	10: Default
3	Short-circuit time (in steps of 1 s) Range: 1....3600 (1....3600s)	1800: Default
4	S0 - R 0: 50Ω 1: 100Ω	1: Default
5	Interface 1..15	0: Default
6	Default 0	0: Reserve
7	Default 0	0: Reserve

7.6.10 Jitter TE

Only available with *jitter* option.

No.	Meaning	Comments
A	0 = TE mode	
B	3 = Jitter module	
C	0 = Measuring mode JITTER (analog)	
1	Power feeding 0: Passive 1: Normal 2: Restricted 3: External	
2	Power feeding voltage in steps of 1/4 volt Range: 40-226 (10 V - 56.5 V)	Only effective if par. no. 1 = normal or restricted
3	Stimulating frame signal 0: 'Binary 1' 1: 'Binary 0' 2: 'Alternating Pattern' 3: 2 EXP 9 -1 4: 2 EXP 11-1 5: 2 EXP 15-1 6: 2 EXP 19-1 7: EXTERNAL B1 8: EXTERNAL B1+B2	
4	Frequency analysis range 0: 2 Hz - 20 kHz 1: 10 Hz - 200 Hz	
5	Evaluation (lower frequency limit) 0: < 1 Hz 1: 5 Hz 2: 10 Hz 3: 15 Hz 4: 30 Hz (CCITT) 5: 50 Hz 6: 80 Hz 7: 110 Hz	
6	Evaluation (upper frequency limit) 0: 40 Hz 1: 270 Hz 2: 350 Hz 3: 600 Hz 4: 1 kHz 5: 3 kHz 6: 10 kHz 7: 20 kHz (CCITT) 8 40 kHz	
7	Measurement 0: Absolute jitter 1: Relative jitter	Only effective if par. no. 13 = 1

8	Reference clock generator 0: System 1: Local	Only effective if par. no. 13 = 1
9	Range select 0: 20 % UIpp 1: 10 % UIpp 2: 5 % UIpp	
10	Jitter frequency 1: 0.1 Hz 2: 0.2 Hz 200.000: 20kHz	Only effective if par. no. 13 = 1
11	Jitter magnitude range 0: 0.35 UIpp 1: 0.7 UIpp	Only effective if par. no. 13 = 1
12	Jitter magnitude 1: 0.004 / 0.002 UIpp 2: 0.008 / 0.004 UIpp 3: 0.012 / 0.006 UIpp 4: 0.016 / 0.008 UIpp ..... 175: 0.700 / 0.350 UIpp	Dependant on par. no. 11 Only effective if par. no. 13 = 1
13	Jitter generator 0: OFF 1: ON	
14	DEFAULT: 0	RESERVE
15	DEFAULT: 0	RESERVE
16	DEFAULT: 0	RESERVE

7.6.11 Jitter NT

Only available with *jitter* option.

No.	Meaning	Comments
A	1 = NT mode	
B	3 = Jitter module	
C	0 = Measuring mode JITTER (analog)	
1	Load 0: Off 1: 25 mW 2: 380 mW 3: 1000 mW 4: External	
2	Transmitted data 0: 'Binary 1' 1: 'Binary 0' 2: 'Alternating Pattern' 3: 2 EXP 9 -1 4: 2 EXP 11-1 5: 2 EXP 13-1 6: 2 EXP 15-1 7: 2 EXP 17-1 8: 2 EXP 19-1	
3	Frequeny analysis range 0: 2 Hz - 20 kHz 1: 10 Hz - 200 Hz	
4	Evaluation (lower limit frequency) 0: < 1 Hz 1: 5 Hz 2: 10 Hz 3: 15 Hz 4: 30 Hz (CCITT) 5: 50 Hz 6: 80 Hz 7: 110 Hz	
5	Evaluation (upper limit frequency) 0: 40 Hz 1: 270 Hz 2: 350 Hz 3: 600 Hz 4: 1 kHz 5: 3 kHz 6: 10 kHz 7: 20 kHz (CCITT) 8 40 kHz	
6	Range select 0: 0.....0.2 UI 1: 0.....0.1 UI 2: 0.....0.05 UI	

7	Jitter frequency 1: 0.1 Hz 2: 0.2 Hz ..... 200.000: 20 kHz	Only effective if par. no. 10 = 1
8	Jitter magnitude range 0: 0.35 UIpp 1: 0.7 UIpp	Only effective if par. no. 10 = 1
9	Jitter magnitude 1: 0.004 / 0.002 UIpp 2: 0.008 / 0.004 UIpp 3: 0.012 / 0.006 UIpp 4: 0.016 / 0.008 UIpp ..... 175: 0.700 / 0.350 UIpp	Dependent on par. no. 8 Only effective if par. no. 10 = 1
10	Jitter generator 0: OFF 1: ON	
11	Clock 0: 15.36 Mhz 1: 12.288 MHz	RESERVE
12	DEFAULT: 0	RESERVE
13	DEFAULT: 0	RESERVE

8 Result structures

Data types

BYTE 8 Bits (MSB.....LSB)

WORD 16 BITS (LOW BYTE, HIGH BYTE)

REAL (floating point - arithmetic) = 32 BITS (Single Precision) (BYTE1, BYTE2,BYTE3, BYTE4)

in the following sequence:

BYTE1=FFFF|FFFF ; BYTE2=FFFF|FFFF; BYTE3=EFFFF|FFFF; BYTE4=SEEE|EEEE

where F = fraction bits, E = exponent bits, S = sign bits

8.1 Electrical characteristics TE

8.1.1 Impedance

Type of measurement	Continuous measurement, 10 x 27 measured values for 1 measurement curve
Type of measured values	Graphical measurement curve (internal format code 0)
Number of bytes (for measured values)	2160
Number of measured value pairs	270
Sequence	$X_1,Y_1,X_2,Y_2.....X_{270},Y_{270}$
Format (all measured values)	REAL, 4 BYTES
Unit of measurement	X = Frequency (Hz), Y = Impedance (Ohm)
Conformance test	Yes, if byte 12 = 2 (only for result)

8.1.2 Unbalance

Type of measurement	Continuous measurement, 10 x 27 measured values for 1 measurement curve
Type of measured values	Graphical measurement curve (internal format code 0)
Number of bytes (for measured values)	2160
Number of measured value pairs	270
Sequence	$X_1,Y_1,X_2,Y_2.....X_{270},Y_{270}$
Format (all measured values)	REAL, 4 BYTES
Unit of measurement	X = Frequency (Hz), Y = Balanced attenuation (dB)
Conformance test	Yes, if byte 15 = 2 (only for result)

8.1.3 Pulse shape

Type of measurement	Continuous measurement, 256 measured values for each measurement curve
Type of measured values	Graphical measurement curve (internal format code 0)
Number of bytes (for measured values)	2048
Number of measured value pairs	256
Sequence	$X_1,Y_1,X_2,Y_2.....X_{256},Y_{256}$
Format (all measured values)	REAL, 4 BYTES
Unit of measurement	X = Time (sec) , Y = Voltage (V)
Conformance test	Yes, if byte 5 = 1,2,3,4 (only for result)

8.1.4 Frame delay

Type of measurement	Continuous measurement
Type of measured values	Numeric single measured values (internal format code 1)
Number of bytes (for measured values)	12
Number of measured values	3
Sequence	Y_1,Y_2,Y_3
Meaning	Y_1 = tmin, $Y_2 = t_{max}$, $Y_3 = t_{avg}$
Format	REAL, 4 BYTES
Unit of measurement	$Y_1=Y_2=Y_3$ in (%)
Conformance test	Automatic

8.1.5 Clock accuracy

Type of measurement	Continuous measurement
Type of measured values	Numeric single measured values (internal format code 1)
Number of bytes (for measured values)	4
Number of measured values	1
Sequence	Y_1
Meaning	Y_1 = df/F
Format	REAL, 4 BYTES
Unit of measurement	Y_1 = in (ppm)
Conformance test	Automatic (only for result)

8.1.6 Impedance of active transmitter

Type of measurement	Continuous measurement
Type of meas. values	Numeric single meas. values (internal format code 1)
Number of bytes (for measured values)	12
No. of meas. values	3
Sequence	Y_1,Y_2,Y_3
Meaning	Y_1 = R(+/-), Y_2 = R(+), Y_3 = R(-)
Format	REAL, 4 BYTES
Unit of measurement	Y_1 = Y_2 = Y_3 in (OHM)
Conformance test	Automatic, (only for result)

8.1.7 Pulse unbalance

Type of measurement	Continuous measurement
Type of meas. values	Numeric single meas. values (internal format code 1)
Number of bytes (for measured values)	4 (if parameter unbalance = area) 8 (if parameter unbalance = amplitude)
Number of measured values	1 (area) 2 (amplitude)
Sequence	Y_1 (area) Y_1, Y_2 (amplitude)
Meaning	Y_1 = dF/Fnom (area) Y_1 = dU+/Unom, Y_2 = dU-/Unom (amplitude)
Format	REAL, 4 BYTES
Unit of measurement	Y_1 = (%) (area) Y_1 = (%), Y_2 = (%) (amplitude)
Conformance test	Automatically on Y_1, (only for result)

8.1.8 Peak current

Type of measurement	Continuous measurement
Type of meas. values	Numeric single meas. values (internal format code 1)
Number of bytes (for measured values)	4
No. of meas. values	1
Sequence	Y_1
Meaning	$Y_1 = I_S$
Format	REAL, 4 BYTES
Unit of measurement	Y_1 = in (A)
Conformance test	Automatic, (only for result)

8.1.9 Jitter

Type of measurement	Continuous measurement
Type of measured values	Numeric single measured values (internal format code 1)
Number of bytes (for measured values)	4
Number of measured values	1
Sequence	Y_1
Meaning	Y_1 = J(UI)
Format	REAL, 4 BYTES
Unit of measurement	Y_1 = in (%)
Conformance test	Automatic, (only for result)

8.1.10 Receiver sensitivity

Type of measurement	Continuous measurement with automatic stop when set measuring time is reached
Structure of measured values	Numeric single measured values (internal format code 4)
Number of bytes (for measured values)	20
Number of measured values	6
Format/meaning (BYTE 0)	Y_1 (BYTE) = statement about conformity of the test (0 = not conformable, FF = conformable, 55 = inconclusive)
Format/meaning (BYTE 1..4)	Y_2 (REAL,SFP) = number of accumulated bit errors
Format/meaning (BYTE 5..8)	Y_3 (REAL,SFP) = measuring time passed (s)
Format/meaning (BYTE 9..12)	Y_4 (REAL,SFP) = bit error rate (BER)
Format/meaning (BYTE 13)	(BYTE) = not relevant
Format/meaning (BYTE 14)	(BYTE) = not relevant
Format/meaning (BYTE 15)	Y_5 (BYTE) = number of correct intervals
Format/meaning (BYTE 16)	Y_6 (BYTE) = number of incorrect intervals
Conformance test	For trace and result

8.2 Electrical characteristics NT

8.2.1 Impedance

Type of measurement	Continuous measurement, 10 x 27 measured values for 1 measurement curve
Type of meas. values	Graphical measurement curve (internal format code 0)
Number of bytes (for measured values)	2160
Number of measured value pairs	270
Sequence	$X_1, Y_1, X_2, Y_2 \ldots\ldots\ldots\ldots X_{270}, Y_{270}$
Format (all measured values)	REAL, 4 BYTES
Unit of measurement	X = Frequency (Hz) , Y = Impedance (Ohm)
Conformance test	Yes, if byte 12 = 2 (only for result)

8.2.2 Unbalance

Type of measurement	Continuous measurement, 10 x 27 measured values for 1 measurement curve
Type of meas. values	Graphical measurement curve (internal format code 0)
Number of bytes (for meas. values)	2160
Number of measured value pairs	270
Sequence	$X_1, Y_1, X_2, Y_2 \ldots\ldots\ldots\ldots X_{270}, Y_{270}$
Format (all measured values)	REAL, 4 BYTES
Unit of measurement	X = Frequency (Hz), Y = Balanced attenuation (dB)
Conformance test	Yes, if byte 15 = 2 (only for result)

8.2.3 Pulse shape

Type of measurement	Continuous measurement, 256 measured values each for one measurement curve
Type of meas. values	Graphical measurement curve (internal format code 0)
Number of bytes (for measured values)	2048
Number of measured value pairs	256
Sequence	X_1,Y_1,Y_2,Y_2.....X_{256},Y_{256}
Format (all measured values)	REAL, 4 BYTES
Unit of measurement	X = Time (sec) , Y = Voltage (V)
Conformance test	Yes, if byte 5 = 1,2,3,4 (only for result)

8.2.4 Impedance of active transmitter

Type of measurement	Continuous measurement
Type of measured values	Numeric single measured values (internal format code 1)
Number of bytes (for measured values)	12
Number of measured values	3
Sequence	Y_1,Y_2,Y_3
Meaning	Y_1 = R(+/-), Y_2 = R(+), Y_3 = R(-)
Format	REAL, 4 BYTES
Unit of measurement	$Y_1 = Y_2 = Y_3$ in (OHM)
Conformance test	Automatic, (only for result)

8.2.5 Peak current

Type of measurement	Continuous measurement
Type of measured values	Numeric single measured values (internal format code 1)
Number of bytes (for measured values)	4
Number of measured values	1
Sequence	Y_1
Meaning	$Y_1 = I_S$
Format	REAL, 4 BYTES
Unit of measurement	Y_1 = in (A)
Conformance test	Automatic, (only for result)

8.2.6 Jitter

Type of measurement	Continuous measurement
Type of measured values	Numeric single measured values (internal format code 1)
Number of bytes (for measured values)	4
Number of measured values	1
Sequence	Y_1
Meaning	Y_1 = J(UI)
Format	REAL, 4 BYTES
Unit of measurement	Y_1 = in (%)
Conformance test	Automatic, (only for result)

8.2.7 Receiver sensitivity

See result structure of measuring mode receiver sensitivity TE.

8.2.8 Receiver input delay characteristics

See result structure of measuring mode receiver sensitivity TE.

8.3 Functional tests TE

8.3.1 Basic interconnection tests

Type of measurement	Continuous measurement with automatic stop when set measuring time is reached
Structure of measured values	Numeric single measured values (internal format code 4)
Number of bytes (for measured values)	20
Number of measured values	6
Format/meaning (BYTE 0)	Y_1 (BYTE) = statement about conformity of the test (0 = not conformable, FF = conformable, 55 = inconclusive)
Format/meaning (BYTE 1..4)	Y_2 (REAL,SFP) = number of accumulated bit errors
Format/meaning (BYTE 5..8)	Y_3 (REAL,SFP) = measuring time expired (s)
Format/meaning (BYTE 9..12)	Y_4 (REAL,SFP) = bit error rate (BER)
Format/meaning (BYTE 13)	Y_5 (BYTE) = statement about activation at beginning of test (0 = not activated, FFH = activated)
Format/meaning (BYTE 14)	Y_6 (BYTE) = statement about deactivation at end of test (0 = not deactivated, FFH = activated)
Conformance test	For trace and result

8.3.2 Organization of frame

Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values (internal format code 5)
Number of bytes (for measured values)	850
Number measured values	1 BYTE (conformity statement) 729 BYTES image design (ASCII - characters) 48 BYTES condensed statement about bit structure (see table)
Format/meaning (BYTE 0)	Y_1 (BYTE) = statement about conformity of the test (0 = not conformable, FF = conformable, 55 = inconclusive)
Format/meaning (BYTE 1..9)	9 BYTE = not relevant
Format/meaning (BYTE 10)	BYTE = X CO-ORDINATE for image design
Format/meaning (BYTE 11)	BYTE = Y CO-ORDINATE for image design
Format/meaning (BYTE 12)	BYTE = number of characters/lines for image design
Format/meaning (BYTE 13)	BYTE = number of lines
Format/meaning (BYTE 14)	BYTE = line spacing in pixels
Format/meaning (BYTE 15)	BYTE = not relevant
Format/meaning (BYTES 16..745)	729 (max) BYTES = ASCII CHARACTERS of the image content (extended)
Format/meaning (BYTES 746..794)	48 BYTE = bit description of the 48 bits of the S_0 frame (table)
Conformance test	For trace and result

No.	Element	Graphical	Result (bit) conform	Result (bit) non-conform
1	zero		**A**	**a**
2	neg		**B**	**b**
3	zero neg		**C**	**c**
4	pos		**D**	**d**
5	pos zero		**E**	**e**
6	pos neg		**F**	**f**
7	pos zero neg		**G**	**g**

8.3.3 TTCN tests APPENDIX B1/B2 TE

Type of measurement	Individual measurements
Structure of measured values	Numeric single measured values (internal format code 6)
Number of bytes (for measured values)	2600
Number of measured values	1 BYTE (conformity statement) max. 988 ASCII characters of display content max. 1530 trace data (ASCII)
Results format	See table below
Conformance test	Only for trace

Detailed results format

Element	Use
0	Y_1 (BYTE) = Statement on conformity of the test (0 = does not conform, 1 = does conform, 2 = inconclusive, 3 = test - with reference to test suite parameters - selected incorrectly)
1...9	9 BYTE = not relevant
10	BYTE = X- COORDINATE for display setup
11	BYTE = Y- COORDINATE for display setup
12	BYTE = Number of characters/lines for display setup
13	BYTE = Number of lines
14	BYTE = Line spacing in pixels
15	BYTE = Not relevant
16...1004	Max. 988 BYTE = ASCII characters of display content
1005...1069	Internally assigned, not relevant
1070 ... 2599	Max. 1530 trace data of the test for trace-analyze program (optional product)

8.4 Functional tests NT

8.4.1 Organization of frame

See results structure of measuring mode organization of frame TE.

8.5 Power feeding tests TE

8.5.1 Power consumption

Description measurement/measured values	
Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values (internal format code 1)
Number of bytes (for measured values)	28
Number of measured values	7
Sequence	$Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7$
Meaning	$Y_1=P_{avg}$, $Y_2=P_{min}$, $Y_3=P_{max}$, $Y_4=I_{avg}$, $Y_5=I_{min}$, $Y_6=I_{max}$, $Y_7=U$
Format	REAL, 4 BYTES
Unit of measurement	Y_1 = (W), Y_2 = (W), Y_3 = (W), Y_4 = (A), Y_5 = (A), Y_6 = (A), Y_7 = (V)
Conformance test	No

8.5.2 Current/time

Description measurement/measured values	
Type of measurement	Individual measurement
Structure of measured values	Graphical measuring curve (internal format code 0)
Number of bytes (for measured values)	1000
Number of measured values	250
Sequence	X_1, Y_1, Y_2, Y_2.....X_{250}, Y_{250}
Format	REAL, 4 BYTES
Unit of measurement	X = time t (sec), Y = current i (A)
Conformance test	No

8.5.3 Power start-up test

Description measurement/measured values	
Type of measurement	Continuous measurement
Structure of measured values	Numeric single measuring values + max 850-byte string (internal format code 2)
Number of bytes (for measured values)	900
Number of measured values	String elements (Power start-up mode = short circuit) 3 + string elements (Power start-up mode = with low voltage)
Sequence	Y_1, Y_2, Y_3 (Power start-up mode = with low voltage)
Meaning	Y_1 = P, Y_2 = I, Y_3 = U (Power start-up mode = with low voltage)
Format	REAL, 4 BYTES (Power start-up mode = with low voltage)
Unit of measurement	Y_1 = (W), Y_2 = (A), Y_3 = (V) (Power start-up mode = with low voltage)
Conformance test	No

Numeric measured values begin with the first byte of the measuring results field. String elements begin with the 50th byte of the measuring results field.

8.5.4 Switchover tests

Description measurement/measured values	
Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values (internal format code 1)
Number of bytes (for measured values)	28
Number of measured values	7
Sequence	$Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7$
Meaning	$Y_1 = P_{avg}$, $Y_2 = P_{min}$, $Y_3 = P_{max}$, $Y_4 = I_{avg}$, $Y_5 = I_{min}$, $Y_6 = I_{max}$, Y_7 = U
Format	Single floating point format (4 BYTES)
Unit of measurement	Y_1 = (W), Y_2 = (W), Y_3 = (W), Y_4 = (A), Y_5 = (A), Y_6 = (A), Y_7 = (V)
Conformance test	Yes

The switchover test is started using this button.

8.5.5 Short interruption

Description measurement/measured values	
Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values (internal format code 2)
Number of bytes (for measured values)	900
Number of measured values	3
Sequence	Y_1, Y_2, Y_3
Meaning	Y_1 = P, Y_2 = I, Y_3 = U
Format	Single floating point format (4 BYTES)
Unit of measurement	Y_1 = (W), Y_2 = (A), Y_3 = (V)
Conformance test	Yes

Numeric measured values begin with the first byte of the measuring results field. String elements begin with the 50th byte of the measuring results field.

8.5.6 Current/transients

Description measurement/measured values	
Type of measurement	Continuous measurement
Structure of measured values	Graphical measuring curve (internal format code 0)
Number of bytes (for measured values)	1000
Number of measured values	250
Sequence	X_1, Y_1, Y_2, Y_2.....X_{250}, Y_{250}
Format	REAL, 4 BYTES
Unit of measurement	X = time t (sec), Y = current i (A)
Conformance test	No

8.6 Power feeding tests NT

The measuring modes switch-on/switchover, overload and load change tests for the power feeding conditions NT are only available as of software version V4.0.

8.6.1 Normal/restricted power output

Type of measurement	Continuous measurement
Structure of measured values	Numeric single values (internal format code 7)
Number of bytes (for measured values)	50
Number measured values	6
Format (only measured values)	REAL, 4 BYTES
Results format	See table below
Conformance test	For trace and result

Detailed results format

BYTE	Application
0	Control byte 0: bytes 2 - 13 are updated 1: bytes 14...25 are updated
1	Number of cycles (0 ...255) (Update depends on parameter setting)
2...5	Present power (output every second)
6...9	Present current (output every second)
10...13	Present voltage (output every second)
14...17	Maximum output per cycle (output at start of new cycle)
18...21	Present current per cycle (output at start of new cycle)
22...25	Present voltage per cycle (output at start of new cycle)
26...49	Reserve

8.6.2 Normal/restricted: switchover tests

Command: `RESULT? [0|1]`

Type of meas.	Continuous measurement
Structure of measured values	Numeric single measured values
No. of bytes (for measured values)	50
Number of measured values	4
Sequence	See below "Detailed results format"
Format	REAL, 4 BYTES
Conformance test	No

Detailed results format

Element	Application
0	Control byte MSB: **0**XXXIXXXX LSB --> Measuring data invalid MSB: **1**XXXIXXX**0** LSB --> Byte 2-13 is current MSB: **1**XXXIXXX**1** LSB --> Byte 2-49 is current
1	Not in use
2 ... 5	Actual power [W]
6 ... 9	Actual current [mA]
10 ... 13	Actual voltage [V]
14 ... 17	Switchover time [ms]
18 ... 49	Not in use

8.6.3 Test type „a“ NT

Command: `RESULT? [0|1]`

Type of meas.	Continuous measurement
Structure of Measured values	Numeric single measured values
No. of bytes (for measured values)	50
Number of measured values	5
Sequence	See "Detailed results format"
Format	REAL, 4 BYTES
Conformance test	No

Detailed results format

Element	Application
0	Control byte MSB: **0**XXXIXXXX LSB --> Measuring data invalid MSB: **1**XXXIXXX**0** LSB --> Byte 2-13 is current MSB: **1**XXXIXXX**1** LSB --> Byte 2-49 is current
1	Not in use
2 ... 5	Actual power [W]
6 ... 9	Actual current [mA]
10 ... 13	Actual voltage [V]
14 ... 17	Time (0...1 V) [ms]
18 ... 21	Time (1...34 V) [ms]
22 ... 49	Not in use

8.6.4 Connecting 1 TE

Command: `RESULT? [0|1]`

Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values
Number of bytes (for measured values)	50
Number of measured values	9
Sequence	See "Detailed results format"
Format	REAL, 4 BYTES
Conformance test	No

Detailed results format

Element	Application

0	`Control byte`
	`MSB: 0XXXIXXXX LSB --> Measuring data invalid`
	`MSB: 1XXXIXXX0 LSB --> Byte 2-13 is current`
	`MSB: 1XXXIXXX1 LSB --> Byte 2-49 is current`

1	Not in use
2 ... 5	Actual power [W]
6 ... 9	Actual current [mA]
10 ... 13	Actual voltage [V]
14 ... 17	Min volt [V] - U (0 ms<t<100 ms) after passing 34 V (+load 50 mA)
18 ... 21	Max volt [V]- U (0 ms<t<100 ms) after passing 34 V (+load 50 mA)
22 ... 25	Avg. min. volt [V] U (0 ms<t<100 ms) after passing 34 V (+load 50 mA)
26 ... 29	Min volt [V] U (0 ms<t<1 s) after change of load (+load 30 mA)
30 ... 33	Max volt [V] U (0 ms<t<1 s) after change of load (+load 30 mA)
34 ... 37	Avg. Min. volt [V] U (0 ms<t<1 s) after change of load (+load 30 mA)
38 ... 49	Not in use

8.6.5 Switch-on response

Command: `RESULT? [0|1]`

Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values
Number of bytes (for measured values)	50
Number of measured values	9
Sequence	See "Detailed results format"
Format	REAL, 4 BYTES
Conformance test	No

Detailed results format

Element	Application
0	Control byte MSB: 0XXXIXXXX LSB --> Measuring data invalid MSB: 1XXXIXXX0 LSB --> Byte 2-13 is current MSB: 1XXXIXXX1 LSB --> Byte 2-49 is current
1	Not in use
2 ... 5	Actual power [W]
6 ... 9	Actual current [mA]
10 ... 13	Actual voltage [V]
14 ... 17	Min volt [V] - U (0 ms<t<100 ms) after passing 30 V
18 ... 21	Max volt [V] U (0 ms<t<100 ms) after passing 30 V
22 ... 25	Avg. min. volt [V] U (0 ms<t<100 ms) after passing 30 V
26 ... 29	Min. volt[V] U (0 ms<t<1 s) after change of load
30 ... 33	Max. volt [V] U (0 ms<t<1 s) after change of load
34 ... 37	Avg. min. volt [V] U (0 ms<t<1 s) after change of load
38 ... 49	Not in use

8.6.6 Restricted (A): at short circuit

Command: `RESULT? [0|1]`

Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values
Number of bytes (for measured values)	50
Number of measured values	6
Sequence	See "Detailed results format"
Format	REAL, 4 BYTES
Conformance test	No

Detailed results format

Element	Application
0	Control byte MSB: **0**XXXIXXXX LSB --> Measuring data invalid MSB: **1**XXXIXXX**0** LSB --> Byte 2-13 is current MSB: **1**XXXIXXX**1** LSB --> Byte 2-49 is current
1	Not in use
2 ... 5	Actual power [W]
6 ... 9	Actual current [mA]
10 ... 13	Actual voltage [V]
14 ... 17	Min. current [mA]
18 ... 21	Max. current [mA]
22 ... 25	Avg. min. current [mA]
26 ... 49	Not in use

8.6.7 Restricted (B): following a short circuit

Command: `RESULT? [0|1]`

Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values
Number of bytes (for measured values)	50
Number of measured values	5
Sequence	See "Detailed results format"
Format	REAL, 4 BYTES
Conformance test	No

Detailed results format

Element	Application

0	`Control byte`
	`MSB: 0XXXIXXXX LSB --> Measuring data invalid`
	`MSB: 1XXXIXXX0 LSB --> Byte 2-13 is current`
	`MSB: 1XXXIXXX1 LSB --> Byte 2-49 is current`

1	Not in use
2 ... 5	Actual power [W]
6 ... 9	Actual current [mA]
10 ... 13	Actual voltage [V]
14 ... 17	Avg. min. current [mA]
18 ... 21	Avg. voltage [V]
22 ... 49	Not in use

8.6.8 Restricted (C): following nominal load

Command: `RESULT? [0|1]`

Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values
Number of bytes (for measured values)	50
Number of measured values	7
Sequence	See "Detailed results format"
Format	REAL, 4 BYTES
Conformance test	No

Detailed results format

Element	Application
0	Control byte MSB: **0**XXXIXXXX LSB --> Measuring data invalid MSB: **1**XXXIXXX**0** LSB --> Byte 2-13 is current MSB: **1**XXXIXXX**1** LSB --> Byte 2-49 is current
1	Not in use
2 ... 5	Actual power [W]
6 ... 9	Actual current [mA]
10 ... 13	Actual voltage [V]
14 ... 17	Voltage [V] - *increasing load, measured at 11 mA*
18 ... 21	Current [mA] - *increasing load, measured at 11 mA*
22 ... 25	Voltage [V] - *increasing load, measured at U> = 34 V*
26 ... 29	Current [mA] - *increasing load, measured at U> = 34 V*
30 ... 49	Not in use

8.6.9 Restricted (D): following capacitive short circuit

Command: `RESULT? [0|1]`

Type of measurement	Continuous measurement
Structure of measured values	Numeric single measured values
Number of bytes (for measured values)	50
Number of measured values	5
Sequence	See "Detailed results format"
Format	REAL, 4 BYTES
Conformance test	No

Detailed results format

Element	Application
0	Control byte MSB: **0**XXXIXXXX LSB --> Measuring data invalid MSB: **1**XXXIXXX**0** LSB --> Byte 2-13 is current MSB: **1**XXXIXXX**1** LSB --> Byte 2-49 is current
1	Not in use
2 ... 5	Actual power [W]
6 ... 9	Actual current [mA]
10 ... 13	Actual voltage [V]
14 ... 17	Time (0 ...1 V) [ms] - increasing load, measured at 11 mA
18 ... 21	Time (1 ...34 V) [ms] - increasing load, measured at 11 mA
22 ... 49	Not in use

8.7 Jitter TE

Command: `RESULT? [0|1]`

Type of measurement	Continuous measurement
Structure of measured values	Own structure (internal format code 3)
Number of bytes (for meas. values)	620
Sequence	See "Detailed results format"
Conformance test	No

Detailed results format

Format/ meaning (BYTE 0)	Number of bar lines in spectrum (binary, 20 or 63)
Format/ meaning (BYTE 1)	0: results are **not** entered 255: results are entered

Format/ meaning (BYTE 2)	`MSB:0000I0000 LSB -> Measuring data valid`
	`MSB:XXXXIXXX1 LSB -> Range 2..50 Hz overmodulated`
	`MSB:XXXXIXX1X LSB -> Range 50..1000 Hz overmodul.`
	`MSB:XXXXIX1XX LSB -> Range 1..20 kHz overmodulated`
	`MSB:XXXXI1XXX LSB -> Range 10..200 Hz overmodulated`
	`MSB:XXX1IXXXX LSB -> Internal information`
	`MSB:XX1XIXXXX LSB -> No new` UI_{pp} `value`
	`MSB:X1XXIXXXX LSB -> No new` UI_{rms} `value`
	`MSB:1XXXIXXXX LSB -> Internal information`

Format/ meaning (BYTE 3)	`MSB:XXXXIXXX1 LSB -> No signal info`
	`MSB:XXXXIXX1X LSB ->` UI_{pp} `value overmodulated`
	`MSB:XXXXIX1XX LSB ->` UI_{pp} `max. value overmodulated`
	`MSB:XXXXI1XXX LSB ->` UI_{rms} `value overmodulated`

Format/meaning (BYTE 4..7)	Y_1 (REAL) = UI % (pp) measured value
Format/meaning (BYTE 8..11)	Y_2 (REAL) = UI % (rms) measured value
Format/meaning (BYTE 12..15)	Y_3 (REAL) = UI % (pp peak hold) measured value
Format/meaning (BYTE 16..275)	Max. 63 (REAL) BAR measured values (only for result)
Format/meaning (BYTE 276..619)	xxx BYTE = At present meaningless
Conformance test	No

8.8 Jitter NT

Type of measurement	Continuous measurement
Structure of meas. values	Individual structure (internal format code 3)
Number of bytes (for meas. values)	620
Number of measured values	See structure
Format/meaning (BYTE 0)	Y_1 (BYTE) = Number of bars for spectrum
Format/meaning (BYTE 1)	Y_2 (BYTE) = Flag whether measured values are valid
Format/meaning (BYTE 2)	Y_3 (BYTE) = Bit structure whether measured values are overmodulated
Format/meaning (BYTE 3)	Y_4 (BYTE) = Bit structure signal recognition
Format/meaning (BYTES 4..7)	Y_5 (REAL) = UI % (pp) measured value
Format/meaning (BYTES 8..11)	Y_6 (REAL) = UI % (rms) measured value
Format/meaning (BYTES 12..15)	Y_7 (REAL) = UI % (pp peak hold) measured value
Format/meaning (BYTES 16..275)	Max. 63 (REAL) BAR measured value (only for result)
Format/meaning (BYTE 276..xxx)	xxx BYTE = At present meaningless
Conformance test	No

9 Appendix

Technical data can be found on the next few pages. There then follows advice on how to program the V.24 printer interface for the K1403. This is concluded by hints on care and maintenance as well details on our service offer.

9.1 Technical data

The technical data of the individual modules are listed after the data for the electrical measurements.

9.1.1 General data

Signal outputs and inputs

S_0 interface	Connection via TAE8+4 or RJ45 (T1D1, CCITT) Configurable in parallel: TE mode and NT mode
Protective ground connection	Safety socket (4 mm, green/yellow) in front panel
Power supply	Internally connected and configurable. Power supply and load to S_0 protected against reversed polarity and overload
Power feeding voltage	Rated voltages ± 40 V Voltage range adjustable from 10 to 56.5 V in steps of 0.25 V
Current	Max. 150 mA at 40 V, short-circuit-proof Current range adjustable with current limiting Voltage range adjustable
Interfaces	V.24 (25-pin) and IEC 625/IEEE 488 (24-pin)

Auxiliary power

Line connection	Protection class 1 (protective ground)	
Line voltage	Nominal range	115 V, 230 V -15 % to +10 %
Line frequency	Nominal range	50 Hz ±5 %, 60 Hz ±5 %
	Limit range of operation	48 to 63 Hz
Power consumption	Approx. 80 VA without options Approx. 120 VA with options	
Protective measures	To DIN VDE 0411	

9.1.2 Environmental conditions

Ambient temperature

Reference value	23 °C ±1 °C
Nominal range	5 to 40 °C
Limit range for storage and transport	-20 to +60 °C

Relative humidity

Reference range at 23 °C	45 to 75 %
Nominal range	20 to 80 % (without condensation)
Limit range of operation	10 to 90 % (without condensation) Absolute humidity < 30 g/m3

Atmospheric pressure

Reference value	101.3 kPa (1013 mbar)
Nominal range	70.0 to 106.0 kPa (700 to 1060 mbar)
Limit range of operation	53.3 to 106.0 kPa (533 to 1060 mbar)
Radio interference suppression	According to assignment 1046/1984
Dimensions (w × h × d)	343 mm × 191 mm × 540 mm

9.1.3 Electrical characteristics

Impedance

General data for transmitter:

Signal shape	Sinusoidal
Frequency range	2 kHz to 1 MHz
Frequency resolution	1 Hz
Frequency setting accuracy	± 2 Hz
Transmitted signal amplitude	U_{rms} = 100 mV to 300 mV
Transmit level accuracy	± 5 % of measured value
Output impedance	< 20 Ω

General data for receiver:

Frequency range	2 kHz ... 1 MHz
Level resolution	12 bits
Receiver bandwidth	< 25 Hz

Output/input impedance:

Measured value indication	Level of impedance in curve form as a function of frequency
Frequency setting range	a) 2 kHz to 1 MHz b) 2 kHz to 40 kHz c) 10 kHz to 200 kHz d) 50 kHz to 1 MHz
Measuring range	100 Ω to 5 kΩ
Measuring error	< 5 % of measured value for 2 kHz ≤ f ≤ 300 kHz < 7 % of measured value for f > 300 kHz
Tolerance system	Fade-in as per CCITT I.430

Impedance of the active transmitter

Measured value display	Internal impedance of the active transmitter when transmitting binary "0"
Measuring range	15 Ω to 25 Ω
Measuring error	± 2 Ω

Unbalance

General data	
Transmitted signal amplitude	700 mV ... 1000 mV otherwise as for impedance measurement
Measured value display	Unbalance attenuation in curve form dependent on frequency
Frequency setting range	a) 2 kHz... 1 MHz b) 80 kHz ... 1 MHz
Measuring range	38 dB ... 78 dB
Insertion loss	2 kHz .. 106 kHz a_e = 0.2 dB ±0.1 dB 106 kHz .. 1 MHz a_e = 0.4 dB ±0.3 dB
Intrinsic unbalance	Up to 300 kHz > 74 dB, otherwise declining at 20 dB/dec
Measuring error	± 0.5dB of the measured value plus the intrinsic unbalance error
Tolerance system	Fade-in as per CCITT I.430

Transmitted signal pulse symmetry

Measured value display	a) numerical indication of the area unbalance b) amplitude unbalance of the 1st and 2nd double pulses
Measuring range	0 % ... ± 10 %
Measuring error	a) Area ± 2.5 % b) Amplitude ± 2 %

Transmitted signal pulse shape

Measured value display	Graphic display of pulse shape dependent on time		
Input impedances	a) 5.6 Ω	± 0.16 Ω	
	b) 50 Ω	± 0.5 Ω	
	c) 400 Ω	± 4 Ω	
Measuring range, single pulse	a) -30 mV ...	+210 mV at	5.6 Ω
	b) -75 mV ...	+825 mV at	50 Ω
	c) -75 mV ...	+2025 mV at	400 Ω
Measuring range, double pulse	a) -225 mV ...	+225 mV at	5.6 Ω
	b) -825 mV ...	+825 mV at	50 Ω
	c) -2025 mV ...	+2025 mV at	400 Ω
Measuring error	a) ± 15 mV		
	b) ± 15 mV		
	c) ± 20 mV		
Level resolution	11 bits plus sign		
Time resolution	Double pulse = 3 * UI ÷ 256 ≙ 0.01 UI ≙ 62.5 ns Single pulse = 2 * UI ÷ 256 ≙ 0.008 UI ≙ 41.7 ns		

Peak current

Measured value display	Numerical display of peak current value
Transmitted frequency	96 kHz, sinusoidal
Transmitted amplitude	Upp = 2.4 V [+ 0 % / - 4%]
Measuring range	0.1 mA .... 1 mA
Measuring error	± 30 µA for i ≤ 600 µA ± 5 % of the measured value for i > 600 µA

Jitter (digital measuring mode in electrical characteristics menu)

Measured value display	Numerical display of jitter amplitude
Transmitted pattern	a) Binary "0" b) Binary "1" c) Alternating pattern "1"/"0AAhex", each in 40 frames d) PN pattern 2^9-1 e) PN pattern 2^{11}-1 f) PN pattern 2^{13}-1 g) PN pattern 2^{15}-1 h) PN pattern 2^{17}-1 i) PN pattern 2^{19}-1
Resolution	0.004 UI = 0.4 % UI
Resolution of display	In steps of 0.4% UI
Measuring range	0 ... 0.5 UI = 50 % UI
Measuring error	a) TE 0.4 % UI b) NT 0.4 % UI + 2 % UI [self-jitter]

Clock accuracy

Measured value display	Numerical display of frequency deviation
Measuring range	-200 ppm ..... +200 ppm
Measuring error	< 10 ppm
Measuring period	1 s, 5 s

Frame delay

Measured value display	Storing and numerical display of the min. and max. frame delay of a TE as well as continuous measured value output
Transmitted pattern	a) Binary "0" b) Binary "1" c) Alternating pattern "1"/"0AAhex", each in 40 frames d) PN pattern 2^9-1 e) PN pattern 2^{11}-1 f) PN pattern 2^{13}-1 g) PN pattern 2^{15}-1 h) PN pattern 2^{17}-1 i) PN pattern 2^{19}-1
Measuring range	± 1 UI = ± 100 % UI
Resolution	0.004 UI = 0.4 % UI
Resolution of display	In steps of 0.4% UI
Measuring error	0.006 UI = 0.6 % UI

9.1.4 Power feeding conditions TE

All characteristic data apply 30 mins after having switched on the device.

The following details apply unless stated otherwise:

Voltage setting range: ±10 V ... 56.5 V, setting accuracy ± 0.7 % based on upper range value of 56.5 V (idle)

Operating modes available: Normal operation, restricted operation

Guaranteed continuous current at ambient temperature of 25°C and within the current range 0 ... 230 mA or 0 ... 250 mA

Voltage	Continuous current
56.5 V	85 mA
50 V	120 mA
45 V	180 mA
40 V	200 mA
32 V	230 mA
24 V	100 mA
10 V	80 mA

Power consumption

Measured value display: Continuous numerical display of the current, voltage and power values

Achievable TE states: Not activated, F2, F3, F4, F5, F6, F7;
as of version 4.0: F7 with ongoing communication

Internal resistance: PS1 feed: ≤ 3.5 Ω
PS2 feed: ≤ 1 Ω (sockets U1, U2)

Current measurement accuracy:
a) 0 ... 230 mA : 1% ± 0.8 mA
b) 0 ... 38 mA : 0.7% ± 120 µA
c) 0 ... 6mA : 0.7% ± 18 µA
d) 0 ... 750µA : 0.7% ± 2.2 µA
e) 0 ... 90 µA : 0.7% ± 1.0 µA

Power measuring accuracy: ≤ 4%, in voltage setting range 24 V ... 56.5 V and in the following current ranges
a) 0 ... 230 mA : 38 mA ... 230 mA
b) 0 ... 38 mA : 6 mA .... 38 mA
c) 0 ... 6 mA : 750 uA ... 6 mA
d) 0 ... 750µA : 90 uA ... 750 µA
e) 0 ... 90 µA : 50uA ... 90 µA

Current/transient measurement

Sampling rate: 5 MHz, 10 MHz, setting accuracy ± 0.1 %

Trigger slope: Positive, negative

Achievable TE states: F3, F4, F5, F6, F7, F8

Current measuring accuracy: 0 ... 70 mA ± 2.5% based on the respective upper limit value

	0 ... 23 mA ± 2.5% based on the respective upper limit value at a capacitive load of CL ≤ 1nF;
Internal resistance	Precision resistor + S0 interface ≤ 18.5 Ω
Trigger setting range	3.0 mA/µs...7.0 mA/µs in 0.5 mA/µs steps with a required settling time of 1 µs; trigger accuracy 0.5 mA/µs

Current/time measurement

Slow sampling:

Current measuring accuracy	0 ... 230 mA, 0 ... 70 mA, ± 1.5% based on respective upper range value; 0 ... 38 mA precision resistor + S0 interface ≤ 18.5 Ω 0 ... 6 mA ± 1.5% based on respective upper range value; precision resistor + S0 interface ≤ 70 Ω 0 ... 750 µA ± 1.5% based on respective upper range value; precision resistor + S0 interface ≤ 1010 Ω; settling time after voltage output: T≤ 100 µs 0 ... 90 µA ± 2.5% based on respective upper range value; precision resistor + S0 interface ≤ 4800 Ω; settling time after voltage output T ≤200 µs The given tolerances for a capacitive load CL ≤ 1 nF apply for the current ranges 0 ... 6 mA, 0 ... 750 µA and 0 ... 90 µA
Time setting range	25 ms to 8 s fixed; setting accuracy 1%

Current/time measurement

Fast sampling:

Current measuring accuracy	0 ... 250 mA, 0 ... 70 mA, ± 2.5% based on respective upper range value; 0 ... 23 mA precision resistor + S0 interface ≤ 18.5 Ω 0 ... 5.5 mA ± 200 µA; precision resistor + S0 interface ≤ 18.5 Ω
As of version 4.0 :	0 ... 5.5 mA-70Ω ± 200 µA; precision resistor + S0 interface ≤ 70 Ω 0 ... 350 µA ± 2% based on respective upper range value ± 10 µA; settling time after voltage output :T ≤ 40µs; precision resistor + S0 interface ≤ 1010Ω

	Unless otherwise mentioned, the voltage settling time is T ≤ 2.5 µs
	In the current measurement ranges 0... 23 mA, 0 ... 5.5 mA (but not 0 ... 5.5 mA 70 Ω) and 0 ... 350 µA the given tolerances apply with a capactive load CL ≤ 1nF.
Sampling rate	0.5 MHz to 10 MHz; setting accuracy ± 0.1 %

Start-up tests

Measured value display	Display of layer 1 protocol (NT states acc. to CCITT rec. I.430)

Start-up tests

Start-up following short circuit:

Voltage setting range	from 25 V to 56.5 V	
Source type		
a) ETS network		
Normal operation.: test a:	Capacity C2	300 µF ± 5%
	Current sink CS	45 mA ± 1 mA
	Current limitation C_L	72 mA ± 1 mA
Normal operation: test b:	Capacity C1, C2	300 µF ± 5%
	Current sink CS	45 mA ± 1 mA
	Current limitation C_L	72 mA ± 1 mA
Rest. operation: test a:	Current limitation CL	9 mA ± 100 µA
Rest. operation: test b:	Capacity C1	300 µF ± 5%
	Current limitation CL	11 mA ± 200 µA
b) Current limitation		
Current setting range	From 1 to 150 mA: Setting accuracy 1 to 45 mA 0.7% ± 30 µA Setting accuracy: 46 mA to 150 mA 1% ± 200 µA	

Start-up tests

Start-up with low voltage:

Measured value display	Additional: numerical display of power consumption, current and PS1 voltage
Resistance	70 Ω ± 1%
Operating mode	Normal

Switchover tests

Measured value display	Numerical display of power consumption, current and PS1 voltage
Mode: normal → restricted	
Measured value display	From SW version 4.0: activation of layer 3 and state messages
Current setting range	From 1 to 30 mA; setting accuracy 0.7% ± 30 µA
Settling time for current limitation	< 3ms
Switchover time	From 5 ms..250 ms, setting accuracy: 1% +- 50 µs, measured at each 50% of the levels
Voltage rise and fall time	< 100 µs, measured at 10% and 90% of the levels
Internal resistance	Normal operation: precision resistor + S0 interface ≤ 3.5 Ω
	Restriced oper.: precision resistor + S0 interface ≤ 18.5 Ω
Mode: restricted → normal	
Switchover time	< 100 µs, measured at 10% and 90% of the levels
Internal resistance and current measurement accuracy apply in restricted operation and 500 ms after voltage switchover	
Internal resistance	a) 0 ... 230 mA: precision resistor + S0 interface ≤ 3.5Ω
	b) 0 ... 70 mA: precision resistor + S0 interface ≤ 18.5Ω
	b) 0 ... 38 mA: precision resistor + S0 interface ≤ 18.5Ω
	c) 0 ... 6 mA: precision resistor + S0 interface ≤ 70 Ω
Current measurement accuracy	a) 0 ... 230 mA: 1% ± 0.8 mA b) 0 ... 70 mA: 0.7% ± 240 µA b) 0 ... 38 mA: 0.7% ± 120 µA c) 0 ... 6 mA: 0.7% ± 18 µA

Short interruption

Interruption time	1 ms...5000 ms; setting accuracy 1% ± 50 µs, measured at each 50% of the levels
Voltage rise and fall time	< 100 µs, measured at 10% and 90% of the levels
Internal resistance	≤ 3.5Ω

Interruption on TEs with detector

Measured value display	Display of layer 1 status via messages, numerical display of power consumption, current and PS1 voltage
Activatable TE states	F4, F6, F7

Voltage dips on TE

Measured value display	Numerical display of power consumption, current and PS1 voltage From SW version 4.0: activation of layer 3 and state messages

9.1.5 Power feeding conditions NT

Measured value display	Running numerical display of current, voltage and power values

Power output

Measured value display	Numerical display of power consumption, current and PS1 or PS2 voltage after completed measurement cycle
Current setting range	1 mA to 300 mA
Current setting accuracy	150 mA ... 300 mA : 1 % ± 1.15 mA 75 mA ... 150 mA : 0.7% ± 600 µA 38 mA ... 75 mA : 0.7 % ± 330 µA 1 mA ... 38 mA : 0.7 % ± 220 µA
Current measurement accuracy	150 mA ... 300 mA : 1% ± 0,8 mA 75 mA ... 150 mA : 0.7 % ± 450 µA 38 mA ... 75 mA : 0.7% ± 230 µA 1 mA ... 38 mA : 0.7 % ± 120 µA
Power measurement accuracy	≤ 4%, in voltage range 24 V ... 56.5 V

Switchover test

Measured value display	Switchover time (single shot)
Current setting range in normal operation	1 mA to 300 mA, Setting accuracy: 1 % ± 1.15 mA
Load resistor in normal-/restricted operation	3.8 kΩ ± 1.5 %
Measurement accuracy of switchover time	1% ± 50 µs, voltage thresholds: 34 V ± 2 %

Switch-on characteristics of NT

Measured value display	Display (single shot) of minimum, maximum and averaged voltages, measured during 0 ms < T < 100 ms period after attaining the S0 voltage 30 V and during 0 ms < T < 1 s after changing the current load.
Current setting range	0 mA to 300 mA, Setting accuracy: 1% ± 1.15 mA

Voltage measurement accuracy ± 0.7 % relative to the upper value 56.5 V (no load)

Overload in restricted operation

Test A: Response during short circuit

Measured value display	Display (single shot) of minimum, maximum and averaged current
Current measurement range	0...38 mA
Current measurement accuracy	0.7% ± 120 µA
Kurzschlußspannung	(3 < 15 mA) ≤ 1V

Test B: Decrease of current load following short circuit

Measured value display	Display (single shot) of the averaged current and voltage
Voltage setting accuracy	± 0.5% ± 500 mV
Current measurement range	0...38 mA
Current measurement accuracy	0.7% ± 120 µA

Voltage measurement accuracy ± 0.7% relative to upper value 56.5 V (no load)

Test C: Increase of current load following nominal load

Measured value display	Display (single shot) of the averaged current and voltage
Current setting range	0...20 mA, setting accuracy: 0.7% ± 220 µA
Current measurement accuracy	0.7% ± 120 µA

Voltage measurement accuracy ± 0.7% relative to upper value 56.5 V (no load)

Test D: Capacitive load following short circuit

Measured value display	Display (single shot) of both rise times
Duration of short circuit	0...60 mins
Source resistance at short	< 7 Ω
Capacity setting range	50 µF...1000 µF, setting accuracy ± 5%
Measurement accuracy of switch-on times	0.5% ± 5 ms

Voltage measurement accuracy ± 0.7% relative to upper value 56.5 V (no load)

Requirements for type "a" NTs

Measured value display	Display (single shot) of both rise times
Duration of short circuit	0...60 mins
Source resistance at short	< 7 Ω
Capacity setting range	50 µF...1000µF, setting accuracy ± 5%
Current setting range	0...300 mA, setting accuracy ± 5%
Measurement accuracy of switch-on times	0.5% ± 5 ms

Voltage measurement accuracy ± 0.7% relative to upper value 56.5 V (no load)

Current change following connection of one TE

Measured value display	Display (single shot) of minimum, maximum and averaged voltages, measured during 0 ms<T<100 ms period after attaining an S0 voltage of 34 V and during 0 ms<T<1 s) after changing the current load.
Current setting range	0 mA to 300 mA, Setting accuracy: 1% ± 1.15 mA

Voltage measurement accuracy ± 0.7% relative to upper value 56.5 V (no load)

9.1.6 IEC interface

Interface functions

SH 1, AH 1, T 6, L 4, TE 0, LE 0, SR 1, RL 0, DC 1, PP 1, DT 1, C0

Multiline interface messages

MLA, MTA, OTA, SPD, SPE, UNL, DCL, SDC, PPC, GET, PPU

Single-line interface messages

ATN, NDAC, NRFD, DAV, IFC, SRQ, EOI

Multiline device messages

DAB, STB, EOS, NUL, PPR

Data transmission

ISO 7-bit code or binary transmission according to DIN IEC 625, IEEE 488 with listener and talker functions.

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9.3 Implemented tests

See *Implemented tests and measurements with K1403.*

9.4 Use of the V.24 interface as printer interface

It is very easy to carry out these connections using so-called V.24/RS 232 adapter boards which are available at specialist shops.

When connecting a printer via a Centronics interface it is necessary to switch a serial-parallel converter and a 25-pin D-Sub socket with a 36-pin Centronics plug between the device and the printer. These converters often already allow for switching over between DATA TERMINAL EQUIPMENT and DATA COMMUNICATION EQUIPMENT so that changes in the pin assignments as described below are not required.

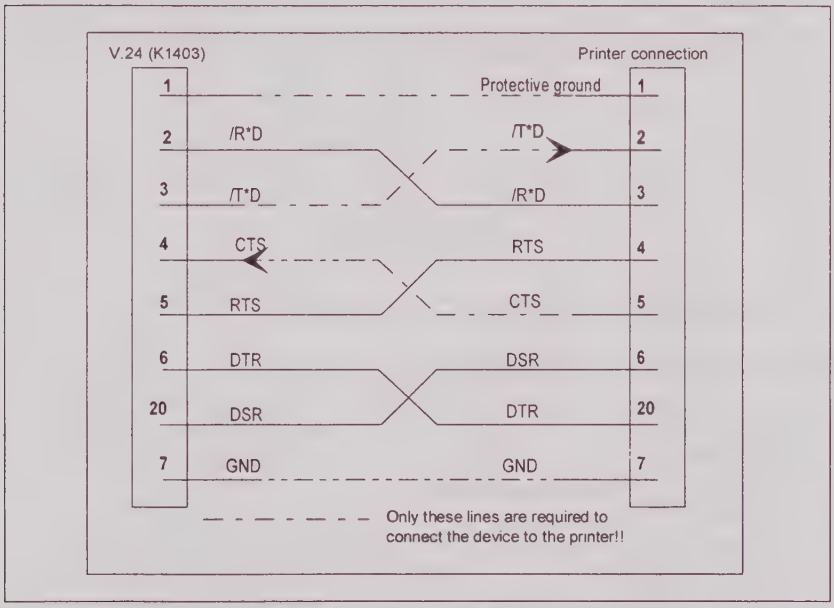

Fig. 9.1: Configuration of connection a of the V.24 interface (K1403 printer)

The serial interface of the K1403 operates to the following specifications:

Baud rate	9600
Data bits	8
Stop bit	1
Parity	Even
Configuration	DTE

If a printer is connected which does not serve the CTS line at pin 4 of the serial interface, the CTS and RTS lines (pin 4 and 5 of the serial interface) can be isolated and pin 4 and 6 of the serial interface connected with each other at the K1403.

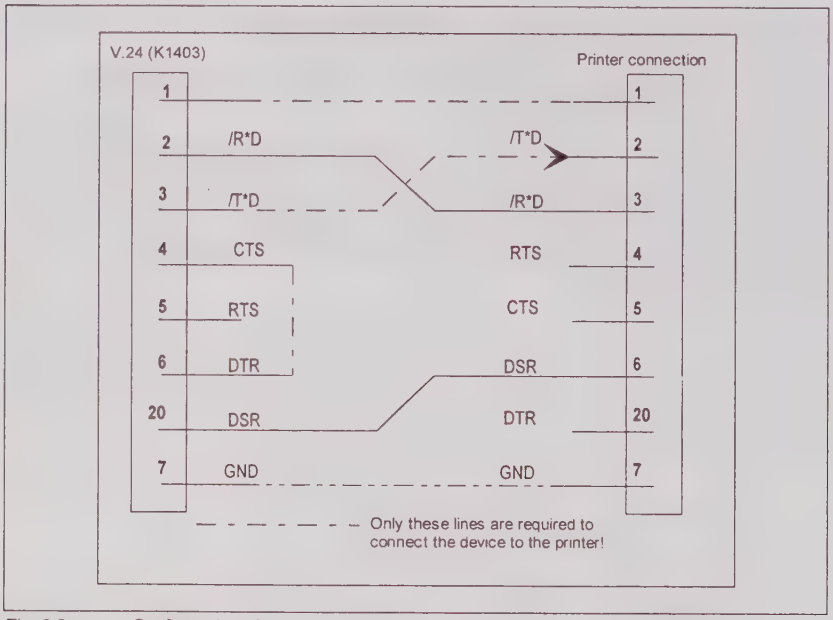

Fig. 9.2: Configuration of connection b of the V.24 interface (K1403 printer)

Connect the K1403 with a 9-pin serial interface of a PC as follows:

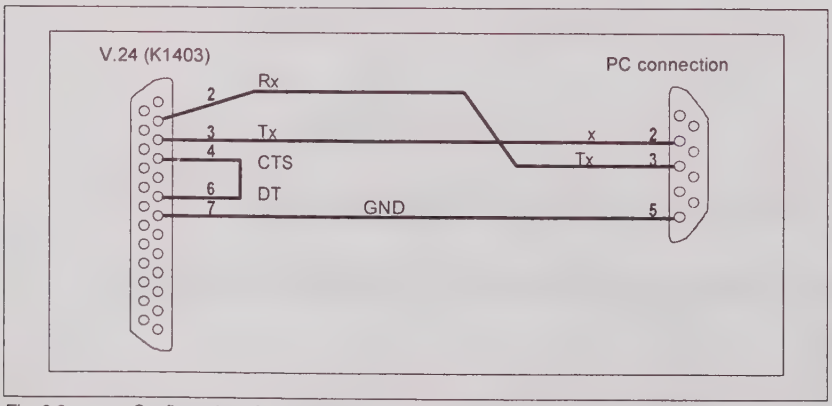

Fig. 9.3: Configuration of connection at the V.24 interface (K1403 9-pin PC serial port)

In the case of a 25-pin serial interface, the following connections apply.

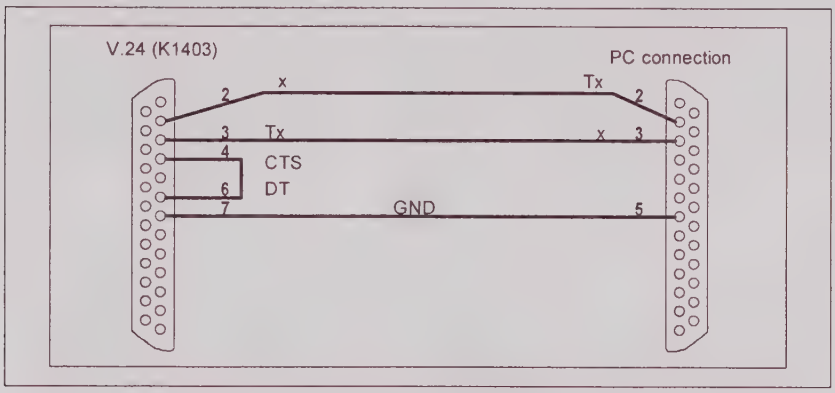

Fig. 9.4: Configuration of connection of the V.24 interface (K1403 25-pin PC serial port)

9.5 Application circuits

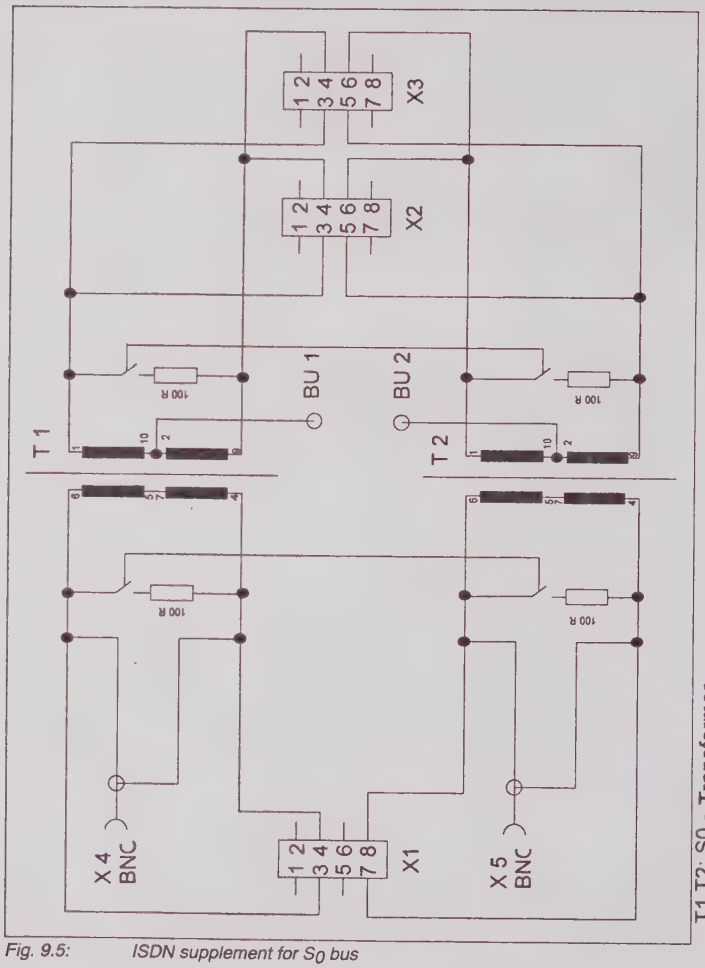

Fig. 9.5: ISDN supplement for S_0 bus

9.6 Care and maintenance

Please observe the following maintenance instructions:

- Prior to cleaning the K1403, switch the device off and disconnect the mains plug.
- All modules contain electrostatically sensitive components. Please observe the necessary safety instructions and ESD protection regulations:

- A dry cloth is sufficient for cleaning the housing surface of K1403. In the event of substantial dirt accumulation, the external parts of the device, the touchscreen and the keys can be cleaned using a cloth soaked in isopropanol. Do not use scouring powder or plastic-solvent cleaning detergents. Cleaning the touchscreen and its border with solvent or abrasive cleaning detergents can lead to malfunction. No fluids may enter the interior of K1403.
- Only a service technician is permitted to clean the housing interior.
- Only authorised personnel are permitted to perform repairs on K1403. Unauthorised opening and improper repairs may cause severe hazards to the user. Please note our service offer below.

Warning!

When operating electrical devices, certain parts of these devices are inevitably under hazardous voltage. Improper handling of these devices may therefore cause death or severe bodily injuries as well as damage to the equipment.

9.6.1 Service offer

Siemens Berlin, AUT 33 S, offers factory servicing for the K1403 ISDN S_0 Analyzer, ensuring that the device is regularly serviced and carefully tested.

This service package includes in detail:

- Cleaning the device
- Checking the general functioning of the equipment
- Adjusting and resetting the specified equipment parameters
- Upgrading the customer equipment HW/SW to current status being supplied
- Continuous test according to new equipment final test

Recommended service intervals: one service per year.

Extension of the service by inclusion of additional device HW/SW by mutual agreement.

Necessary repairs are carried out immediately upon notification. If the device warranty has expired, the accumulated spare parts and repairing costs will be billed separately.

Should you have to return your K1403 to Siemens Service for repair, please remember to include a completed returned goods accompanying note - it always receives our prompt attention. You will find it in the brochure entitled "Before you begin".

SIEMENS

Implemented Tests and Measurements with K1403

Tabellarische Zusammenstellung/List of Tests Bestell-Nr./Order No.: C73000-T6074-C53-2

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Das im vorliegenden Handbuch beschriebene Produkt stimmt mit den Vorschriften des Gesetzes über die elektromagnetische Verträglichkeit von Geräten (EMVG) bzw. den Vorschriften der Richtlinie des Rates vom 03.05.1989 zur Angleichung der Rechtsvorschriften der Mitgliedstaaten über die elektromagnetische Verträglichkeit (89/336/EWG) überein.

The product described in this manual complies with the statutory regulations on electromagnetic compatibility of devices (EMC) or the regulations of the guideline of the council from 03.05.1989 for adaptation of the statutory regulations of the member countries on electromagnetic compatibility of devices (89/336/EEC).

Hinweis

Mit den nachfolgenden Tabellen ist eine Auflistung der Tests und Messungen in der Schicht-1 der ISDN-S_0-Schnittstelle gegeben. Dabei wird für jeden Test der Bezug zur entsprechenden Richtlinie ETSI 300_012, CTS-2 sowie NET3 aufgeführt. In der Kommentarspalte sind für den K1403

* durch Schattierung die nicht implementierten Messungen in der vorliegenden Geräteversion und

* die Ausführung der Messart

beschrieben. Für das Grundgerät werden

* Erweiterungen mit den Optionen "Kabelnachbildung" **[SIM-LHC]**, **[SIM-HC]**[1], "Analoge Tests" **[AN]** und "Jitter-Messung" **[JIT]**

angeboten.

Weitere Informationen erhalten Sie von Ihrer nächsten SIEMENS-Niederlassung.

Note

With the following list a summary of the tests and measurements on layer-1 of the ISDN-S_0-interface is given. For each test the corresponding recommendation ETSI 300_012, CTS- 2 and NET3 is quoted. In the comment column

* the not implemented tests in the present version of K1403 are shaded grey and

* the implementation of the test is described.

The upgrade with the not implemented tests will be done only by replacing EPROMs. For extension of the basic unit

* the optional add-on-boards "cable simulator" **[SIM-LHC]**,**[SIM-HC]**[2], "analogue tests" **[AN]** and "jitter measurement" **[JIT]**

are offered.

For further information please contact your local SIEMENS sales office.

---

[1] HC : hoch kapazitives Kabel } 1 Steckbaugruppe
LHC : nieder und hoch kapazitives Kabel } 1 Steckbaugruppe

[2] HC : high capacitive cable } 1 add-on board
LHC : low and high capacitive cable } 1 add-on board

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1 TESTS ON TE

1.1 BASIC INTERCONNECTION TESTS

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
1.1	Basic interconnection test without noise, point to point configuration (high cap. cable with 6dB attenuation)	D.1	--	2	[SIM-HC] config. I
1.2	Basic interconnection test without noise, short passive bus configuration (high cap. cable with 2µs delay) with 8TEs (including the TE under test) clustered at the far end of the bus	D.1	--	2	[SIM-HC] config. II
1.3	Basic interconnection test without noise, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source	D.1	--	2	[SIM-LHC] config. IIIa
1.4	Basic interconnection test without noise, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source	D.1	--	2	[SIM-HC] config. IIIb
1.5	Basic interconnection test without noise, ideal configuration (direct connection UUT-TE to NT)	D.1	--	2	config. IV
1.6	Basic interconnection test with 200kHz sine wave noise, point to point configuration (high cap. cable with 6dB attenuation)	D.1	--	2	[SIM-HC] config. I
1.7	Basic interconnection test with 2MHz sine wave noise, point to point configuration (high cap. cable with 6dB attenuation)	D.1	--	2	[SIM-HC] config. I
1.8	Basic interconnection test with 200kHz sine wave noise, short passive bus configuration (high cap. cable with 2µs delay) with 8TEs (including the TE under test) clustered at the far end of the bus	D.1	--	2	[SIM-HC] config. II
1.9	Basic interconnection test with 2MHz sine wave noise, short passive bus configuration (high cap. cable with 2µs delay) with 8TEs (including the TE under test) clustered at the far end of the bus	D.1	--	2	[SIM-HC] config. II
1.10	Basic interconnection test with 200kHz sine wave noise, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source	D.1	--	2	[SIM-HC] config. IIIa
1.11	Basic interconnection test with 2MHz sine wave noise, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source	D.1	--	2	[SIM-HC] config. IIIa
1.12	Basic interconnection test with 200kHz sine wave noise, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source	D.1	--	2	[SIM-LHC] config. IIIb
1.13	Basic interconnection test with 2MHz sine wave noise, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source	D.1	--	2	[SIM-LHC] config. IIIb

1.2 BINARY ORGANISATION OF FRAME

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
2.1	Binary organisation of INFO3 frames, B1&B2 channels filled with 2^9-1 PRBS	D.2.1.1	5.4.2.1	4.1.1	
2.2	Binary organisation of INFO1 frames	D.2.1.2	6.2.2	4.1.2	

1.3 D CHANNEL ACCESS CONTROL PROCEDURE

1.3.1 Appendix B1

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment / Testname
3.1	Inter frame (layer 2) time fill of the D channel from the TE for priority class 1	D.3.1.1	6.1.1	5.1.1	F7/DCBinaryOneCL1
3.2	Inter frame (layer 2) time fill of the D channel from the TE for priority class 2	D.3.1.1	6.1.1	5.1.1	F7/DCBinaryOneCL2
3.3	D-echo channel response: Mismatch at the normal priority level. Immediate stop of transmission by the TE when detecting an error on the D channel (sending 0 and echoed 1) for priority class 1	D.3.1.2a	6.1.5	5.1.2a	F7/DCNormalPL0CL1
3.4	D-echo channel response: Mismatch at the normal priority level. Immediate stop of transmission by the TE when detecting an error on the D channel (sending 0 and echoed 1) for priority class 2	D.3.1.2a	6.1.5	5.1.2a	F7/DCNormalPL0CL2
3.5	D-echo channel response: Mismatch at the normal priority level. Immediate stop of transmission by the TE when detecting an error on the D channel (sending 1 and echoed 0) for priority class 1	D.3.1.2a	6.1.5	5.1.2a	F7/DCNormalPL1CL1
3.6	D-echo channel response: Mismatch at the normal priority level. Immediate stop of transmission by the TE when detecting an error on the D channel (sending 1 and echoed 0) for priority class 2	D.3.1.2a	6.1.5	5.1.2a	F7/DCNormalPL1CL2
3.7	D-echo channel response: Respect by the TE of the priority class 1, after an error has occurred in the D-echo channel, wait for 8 continuous D-echo channel bits set to binary one before sending a subsequent layer 2 frame	D.3.1.2b	6.1.4	5.1.2b	F7/DCPriorityClass1
3.8	D-echo channel response: Respect by the TE of the priority class 2, after an error has occurred in the D-echo channel, wait for 10 continuous D-echo channel bits set to binary one before sending a subsequent layer 2 frame	D.3.1.2b	6.1.4	5.1.2b	F7/DCPriorityClass2
3.9	D-echo channel response: Respect by the TE of its priority level for priority class 1, after a successful transmission of a layer 2 frame, wait for 9 continuous D-echo channel bits set to binary one before sending a subsequent layer 2 frame	D.3.1.2c	6.1.4	5.1.2c	F7/DCNormtoLowPLCL1

3.10	D-echo channel response: Respect by the TE of its priority level for priority class 2, after a successful transmission of a layer 2 frame, wait for 11 continuous D-echo channel bits set to binary one before sending a subsequent layer 2 frame	D.3.1.2c	6.1.4	5.1.2c	F7/DCNormtoLowPLCL2
3.11	D-echo channel response: Respect by the TE of its priority level for priority class 1, if no layer 2 frame is available wait for 9 continuous D-echo channel bits set to binary one before changing back to the normal priority level	D.3.1.2c	6.1.4	5.1.2c	F7/DCLowtoNormPLCL1
3.12	D-echo channel response: Respect by the TE of its priority level for priority class 2, if no layer 2 frame is available wait for 11 continuous D-echo channel bits set to binary one before changing back to the normal priority level	D.3.1.2c	6.1.4	5.1.2c	F7/DCLowtoNormPLCL2

no. 3.3 -3.12

L2-, L3-protocol for basic call functions according to CTS2-ISDN-Basic Access Appendix B2

1.3.2 Appendix B2

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment / Testname
3.13	To check that IUT doesn't bufferize layer 2 frames ID_REQ when D-channel is blocked	D.3.1.2a	6.2.3.2		CP/F7/CPF7DBLK_TEI
3.14	To check that IUT doesn't bufferize layer 2 frames SABME when D-channel is blocked	D.3.1.2a	6.2.3.2		CP/F7/CPF7DBLK_SABME
3.15	To check that IUT doesn't bufferize layer 3 frames SETUP when D-channel is blocked	D.3.1.2a	6.2.3.2		CP/F7/CPF7DBLK_SETUP
3.16	To check that IUT doesn't bufferize layer 3 frames DISC when D-channel is blocked	D.3.1.2a	6.2.3.2		CP/F7/CPF7DBLK_DISC

1.4 ACTIVATION / DEACTIVATION PROCEDURE

1.4.1 Appendix B1

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment / Testname
4.1	Act.-/Deactivation procedure when power is applied in state F1	D.3.2.1 (1a)	6.2	5.2.(1)	F1/AD1aF1_PS&LP-on
4.2	Act.-/Deactivation procedure when power is applied in state F1.0	D.3.2.1 (1b)	6.2	5.2.(1)	F10/AD1bF10_LP-on
4.3	Act.-/Deactivation procedure when loss of power in state F1.1	D.3.2.1 (1c)	6.2		F11/AD1cF11_LP-off
4.4	Act.-/Deactivation procedure when power is applied in state F1.1	D.3.2.1 (1d)	6.2	5.2.(2)	F11/AD1dF11_PS-on
4.5	Act.-/Deactivation procedure when T3 expires in state F1.1	D.3.2.1 (2)	6.2		F1/AD2F11_CHK_T3
4.6	Act.-/Deactivation procedure when loss of power PS in state F2	D.3.2.1 (3a)	6.2	5.2.(3)	F2/AD3aF2_PS-off
4.7	Act.-/Deactivation procedure when loss of local power in state F2	D.3.2.1 (3b)	6.2	5.2.(3)	F2/AD3bF2_LP-off
4.8	Act.-/Deactivation procedure when receiving INFO0 in state F2	D.3.2.1 (4)	6.2	5.2.(4)	F2/AD4F2_RX-I0
4.9	Act:-/Deactivation procedure when receiving INFO2 in state F2	D.3.2.1 (5)	6.2	5.2.(5)	F2/AD5F2_RX_I2
4.10	Act.-/Deactivation procedure when receiving INFO4 in state F2	D.3.2.1 (6)	6.2	5.2.(6)	F2/AD6F2_RX_I4
4.11	Act.-/Deactivation procedure when receiving INFOx in state F2	D.3.2.1 (7)	6.2		F2/AD7F2_RX-IX
4.12	Act.-/Deactivation procedure when T3 expires in state F2	D.3.2.1 (8)	6.2		F2/AD8F2_CHK_T3
4.13	Act.-/Deactivation procedure when loss of power PS in state F3	D.3.2.1 (9a)	6.2	5.2.(7)	F3/AD9aF3_PS-off
4.14	Act.-/Deactivation procedure when loss of local power in state F3	D.3.2.1 (9b)	6.2	5.2.(7)	F3/AD9bF3_LP-off
4.15	Act.-/Deactivation procedure when receiving PH-AR in state F3	D.3.2.1 (10)	6.2	5.2.(8)	F3/AD10F3_PH-AR
4.16	Act.-/Deactivation procedure when receiving INFO0 in state F3	D.3.2.1 (11)	6.2		F3/AD11F3_RX_I0
4.17	Act.-/Deactivation procedure when receiving INFO2 in state F3	D.3.2.1 (12)	6.2	5.2.(9)	F3/AD12F3_RX_I2
4.18	Act.-/Deactivation procedure when receiving INFO4 in state F3	D.3.2.1 (13)	6.2	5.2.(10)	F3/AD13F3_RX_I4
4.19	Act.-/Deactivation procedure when receiving INFOx in state F3	D.3.2.1 (14)	6.2		F3/AD14F3_RX_IX
4.20	Act.-/Deactivation procedure when T3 expires in state F3	D.3.2.1 (15)	6.2		F3/AD15F3_CHK_T3
4.21	Act.-/Deactivation procedure when loss of power PS in state F4	D.3.2.1 (16a)	6.2	5.2.(11)	F4/AD16aF4_PS-off
4.22	Act.-/Deactivation procedure when loss of local power in state F4	D.3.2.1 (16b)	6.2	5.2.(11)	F4/AD16bF4_LP-off
4.23	Act.-/Deactivation procedure when receiving INFO0 in state F4	D.3.2.1 (17)	6.2		F4/AD17F4_RX_I0
4.24	Act.-/Deactivation procedure when receiving INFO2 in state F4	D.3.2.1 (18)	6.2	5.2.(13)	F4/AD18F4_RX_I2

4.25	Act.-/Deactivation procedure when receiving INFO4 in state F4	D.3.2.1 (19)	6.2	5.2.(13)	F4/AD19F4_RX_I4
4.26	Act.-/Deactivation procedure when receiving INFOx in state F4	D.3.2.1 (20)	6.2		F4/AD20F4_RX_IX
4.27	Act.-/Deactivation procedure when T3 expires in state F4	D.3.2.1 (21)	6.2	5.2.(12)	F4/AD21F4_CHK_T3
4.28	Act.-/Deactivation procedure when loss of power PS in state F5	D.3.2.1 (22a)	6.2	5.2.(14)	F5/AD22aF5_PS-off
4.29	Act.-/Deactivation procedure when loss of local power in state F5	D.3.2.1 (22b)	6.2	5.2.(14)	F5/AD22bF5_LP-off
4.30	Act.-/Deactivation procedure when receiving INFO0 in state F5	D.3.2.1 (23)	6.2		F5/AD23F5_RX_I0
4.31	Act.-/Deactivation procedure when receiving INFO2 in state F5	D.3.2.1 (24)	6.2	5.2.(16)	F5/AD24F5_RX_I2
4.32	Act.-/Deactivation procedure when receiving INFO4 in state F5	D.3.2.1 (25)	6.2	5.2.(17)	F5/AD25F5_RX_I4
4.33	Act.-/Deactivation procedure when receiving INFOx in state F5	D.3.2.1 (26)	6.2		F5/AD26F5_RX_IX
4.34	Act.-/Deactivation procedure when T3 expires in state F5	D.3.2.1 (27)	6.2	5.2.(15)	F5/AD27F5_CHK_T3
4.35	Act.-/Deactivation procedure when loss of power PS in state F6	D.3.2.1 (28a)	6.2	5.2.(18)	F6/AD28aF6_PS-off
4.36	Act.-/Deactivation procedure when loss of local power in state F6	D.3.2.1 (28b)	6.2	5.2.(18)	F6/AD28bF6_LP-off
4.37	Act.-/Deactivation procedure when loss of power PS in state F6	D.3.2.1 (28c)	6.2	5.2.(18)	F6/AD28cF6_PS-off
4.38	Act.-/Deactivation procedure when loss of framing in state F6	D.3.2.1 (29)	6.2	5.2.(22)	F6/AD29F6_Lostfr
4.39	Act.-/Deactivation procedure when receiving PH-AR in state F6	D.3.2.1 (30)	6.2		F6/AD30F6_PH_AR
4.40	Act.-/Deactivation procedure when receiving INFO0 in state F6	D.3.2.1 (31)	6.2	5.2.(20)	F6/AD31F6_RX_I0
4.41	Act.-/Deactivation procedure when receiving INFO2 in state F6	D.3.2.1 (32)	6.2		F6/AD32F6_RX_I2
4.42	Act.-/Deactivation procedure when receiving INFO4 in state F6	D.3.2.1 (33)	6.2	5.2.(21)	F6/AD33F6_RX_I4
4.43	Act.-/Deactivation procedure when T3 expires in state F6	D.3.2.1 (34)	6.2	5.2.(19)	F6/AD34F6_CHK_T3
4.44	Act.-/Deactivation procedure when loss of power PS in state F7	D.3.2.1 (35a)	6.2	5.2.(23)	F7/AD35aF7_PS-off
4.45	Act.-/Deactivation procedure when loss of local power in state F7	D.3.2.1 (35b)	6.2	5.2.(23)	F7/AD35bF7_LP-off
4.46	Act.-/Deactivation procedure when loss of power PS in state F7	D.3.2.1 (35c)	6.2	5.2.(23)	F7/AD35cF7_PS-off
4.47	Act.-/Deactivation procedure when loss of framing in state F7	D.3.2.1 (36)	6.2	5.2.(26)	F7/AD36F7_Lostfr
4.48	Act.-/Deactivation procedure when receiving INFO0 in state F7	D.3.2.1 (37)	6.2	5.2.(24)	F7/AD37F7_RX_I0
4.49	Act.-/Deactivation procedure when receiving INFO2 in state F7	D.3.2.1 (38)	6.2	5.2.(25)	F7/AD38F7_RX_I2
4.50	Act.-/Deactivation procedure when receiving INFO4 in state F7	D.3.2.1 (39)	6.2		F7/AD39F7_RX_I4

4.51	Act.-/Deactivation procedure when loss of power PS in state F8	D.3.2.1 (40a)	6.2	5.2.(27)	F8/AD40aF8_PS-off
4.52	Act.-/Deactivation procedure when loss of local power in state F8	D.3.2.1 (40b)	6.2	5.2.(27)	F8/AD40bF8_LP-off
4.53	Act.-/Deactivation procedure when receiving PH-AR in state F8	D.3.2.1 (41)	6.2		F8/AD41F8_PH-AR
4.54	Act.-/Deactivation procedure when receiving INFO0 in state F8	D.3.2.1 (42)	6.2		F8/AD42F8_RX-I0
4.55	Act.-/Deactivation procedure when receiving INFO2 in state F8	D.3.2.1 (43)	6.2	5.2.(28)	F8/AD43F8_RX-I2
4.56	Act.-/Deactivation procedure when receiving INFO4 in state F8	D.3.2.1 (44)	6.2	5.2.(29)	F8/AD44F8_RX-I4
4.57	Act.-/Deactivation procedure when receiving INFOx in state F8	D.3.2.1 (45)	6.2		F8/AD45F8_RX-IX
4.58	Act.-/Deactivation procedure when T3 expires in state F8	D.3.2.1 (46)	6.2		F8/AD46F8_CHK_T3

1.4.2 Appendix B2

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment / Test name
4.59	To check that IUT is brought to state F3 when receiving Info 0 in state F2 and that it sends a MPH-II(c) primitive to ask for a TEI	D.3.2.1 (B2-4)	6.2		CP/F2/CPF2MPHIICI0
4.60	To check that IUT is brought to state F6 when receiving Info 2 in state F2 and that it sends a MPH-II(c) primitive to ask for a TEI	D.3.2.1 (B2-5)	6.2		CP/F2/CPF2MPHIICI2
4.61	To check that IUT is brought to state F7 when receiving Info 4 in state F2 and that it sends a MPH-II(c) primitive to ask for a TEI	D.3.2.1 (B2-6a)	6.2		CP/F2/CPF2MPHIICI4
4.62	To check that IUT is brought to state F7 when receiving Info 4 in state F2 and that it sends a PH-AI primitive	D.3.2.1 (B2-6b)	6.2		CP/F2/CPF2PHAI
4.63	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPH-II(d) primitive	D.3.2.1 (B2-9)	6.2		CP/F3/CPF3MPHIID
4.64	To check that IUT doesn't set on a layer 2 timer in the same time as T3	D.3.2.1 (B2-10)	6.2		CP/F4/CPF4Tlayer2
4.65	To check that IUT is brought to state F7 when receiving Info 4 in state F4 and that a PH-AI primitive is sent	D.3.2.1 (B2-13)	6.2		CP/F3/CPF3PHAI
4.66	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPH-II(d) primitive	D.3.2.1 (B2-16)	6.2		CP/F4/CPF4MPHIID
4.67	To check that IUT is brought to state F7 when receiving Info 4 in state F4 and that a PH-AI primitive is sent	D.3.2.1 (B2-19)	6.2		CP/F4/CPF4PHAI
4.68	To check that IUT sends a PH-DI on T3 expiration	D.3.2.1 (B2-21)	6.2		CP/F4/CPF4PHDI_T3exp
4.69	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPH-II(d) primitive	D.3.2.1 (B2-22)	6.2		CP/F5/CPF5MPHIID
4.70	To check that IUT has no action on receipt of Info 0 in state F5	D.3.2.1 (B2-23)	6.2		CP/F5/CPF5PHDI_I0T3

4.71	To check that IUT is brought to state F7 when receiving Info 4 in state F4 and that a PH-AI primitive is sent	D.3.2.1 (B2-25)	6.2		CP/F5/CPF5PHAI
4.72	To check that IUT sends a PH-DI on T3 expiration	D.3.2.1 (B2-27a)	6.2		CP/F5/CPF5PHDI_T3expa
4.73	To check that IUT sends a PH-DI on T3 expiration	D.3.2.1 (B2-27b)	6.2		CP/F5/CPF5PHDI_T3expb
4.74	To check that a PH-AR generates no action from IUT in state F6 but has really been sent	D.3.2.1 (B2-30a)	6.2		CP/F6/CPF6PHARa
4.75	To check that a PH-AR generates no action from IUT in state F6 but has really been sent	D.3.2.1 (B2-30b)	6.2		CP/F6/CPF6PHARb
4.76	To check that IUT goes from F6 to F3 on receipt of I0 while T3 is set on	D.3.2.1 (B2-31a)	6.2		CP/F6/CPF6PHDI_I0T3
4.77	To check that IUT does send a PH-DI primitive upon receipt of Info 0 in state F6	D.3.2.1 (B2-31b)	6.2		CP/F6/CPF6PHDI_I0
4.78	To check that IUT is brought to state F7 when receiving Info 4 in state F6 and that a PH-AI primitive is sent	D.3.2.1 (B2-33a)	6.2		CP/F6/CPF6PHAIa
4.79	To check that IUT is brought to state F7 when receiving Info 4 in state F6 during T3 and that a PH-AI primitive is sent	D.3.2.1 (B2-33b)	6.2		CP/F6/CPF6PHAIb
4.80	To check that IUT sends a PH-DI on T3 expiration	D.3.2.1 (B2-34)	6.2		CP/F6/CPF6PHDI_T3exp
4.81	To check MPH-EI primitives on receipt of Info X and then Info 4	D.3.2.1 (B2-36a)	6.2		CP/F7/CPF7MPHEI_IX
4.82	To check MPH-EI primitives on receipt of Info X and then Info 2	D.3.2.1 (B2-36b)	6.2		CP/F7/CPF7MPHEI_IXI2
4.83	To check MPH-EI and PH-DI primitives on receipt of Info X and then Info 0	D.3.2.1 (B2-36c)	6.2		CP/F7/CPF7MPHEI_IXI0
4.84	To check MPH-EI and PH-DI primitives on receipt of Info X and then Info 2 and Info 0	D.3.2.1 (B2-36d)	6.2		CP/F7/CPF7MPHEI_IXI2I0
4.85	To watch consequenses of a layer 1 disturbance on layer 2 when IUT doesn't use T309	D.3.2.1 (B2-36e)	6.2		CP/F7/CPF7BUFa_IX
4.86	To watch consequenses of a layer 1 disturbance on layer 2 when IUT uses T309	D.3.2.1 (B2-36f)	6.2		CP/F7/CPF7BUFb_IX
4.87	To check that IUT does send a PH-DI primitive upon receipt of Info 0 in state F7	D.3.2.1 (B2-37)	6.2		CP/F7/CPF7PHDI_I0
4.88	To check MPH-EI primitives on receipt of Info 2 and then Info 4	D.3.2.1 (B2-38a)	6.2		CP/F7/CPF7MPHEI_I2
4.89	To check MPH-EI primitives on receipt of Info 2 and then Info X	D.3.2.1 (B2-38b)	6.2		CP/F7/CPF7MPHEI_I2IX
4.90	To check MPH-EI and PH-DI primitives on receipt of Info 2 and then Info 0	D.3.2.1 (B2-38c)	6.2		CP/F7/CPF7MPHEI_I2I0
4.91	To check MPH-EI and PH-DI primitives on receipt of Info 2 and then Info X and Info 0	D.3.2.1 (B2-38d)	6.2		CP/F7/CPF7MPHEI_I2IXI0
4.92	To watch consequenses of a layer 1 disturbance on layer 2 when IUT doesn't use T309	D.3.2.1 (B2-38e)	6.2		CP/F7/CPF7BUFa_I2
4.93	To watch consequenses of a layer 1 disturbance on layer 2 when IUT uses T309	D.3.2.1 (B2-38f)	6.2		CP/F7/CPF7BUFb_I2
4.94	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPH-II(d) primitive	D.3.2.1 (B2-40a)	6.2		CP/F8/CPF8MPHIIDa

4.95	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPH-II(d) primitive	D.3.2.1 (B2-40b)	6.2		CP/F8/CPF8MPHIIDb
4.96	To check that a PH-AR generates no action from IUT in state F8 but has really been sent	D.3.2.1 (B2-41a)	6.2		CP/F8/CPF8PHARa
4.97	To check that a PH-AR generates no action from IUT in state F8 but has really been sent	D.3.2.1 (B2-41b)	6.2		CP/F8/CPF8PHARb
4.98	To check that IUT goes from F8 to F3 on receipt of I0 while T3 is set on	D.3.2.1 (B2-42a)	6.2		CP/F8/CPF8PHDI_I0T3
4.99	To check that IUT does send a PH-DI primitive upon receipt of Info 0 in state F8	D.3.2.1 (B2-42b)	6.2		CP/F8/CPF8PHDI_I0b
4.100	To check that IUT is brought to state F7 when receiving Info 4 in state F8 and that a PH-AI primitive is sent	D.3.2.1 (B2-44b)	6.2		CP/F8/CPF8PHAIb
4.101	To check that IUT is brought to state F7 when receiving Info 4 in state F8 during T3 and that a PH-AI primitive is sent	D.3.2.1 (B2-44c)	6.2		CP/F8/CPF8PHAIc
4.102	To check that IUT returns to state F3 on T3 expiration	D.3.2.1 (B2-46)	6.2		CP/F8/CPF8PHDI_T3exp

1.5 TIMERS FOR ACTIVATION / DEACTIVATION

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment / Test name
5.1	Timer for activation when receiving INFO2 in state F3 (Test A)	D.3.2.2.1.1	6.2.6.1		F3/TIF3Info2
5.2	Timer for activation when receiving inverted INFO2 in state F3				F4/TIF3Info2_inv
5.3	Timer for activation when receiving INFO4 in state F3 Test A	D.3.2.2.2.1	6.2.6.1		F3/TIF3Info4
5.4	Timer for activation when receiving INFO2 in state F4 (Test B)	D.3.2.2.1.2	6.2.6.1		F4/TIF4Info2
5.5	Timer for activation when receiving INFO4 in state F4 (Test B)	D.3.2.2.2.2	6.2.6.1		F4/TIF4Info4
5.6	Timer for activation when receiving any signal	D.3.2.2.3	6.2.6.1		F4/TIF4InfoX
5.7	Value of timer T3	D.3.2.2.4	6.2.5		F3/TItimerT3
5.8	Timer for physical deactivation in state F6 Test A	D.3.2.2.5.1	6.2.7		F6/TIF6physdeact
5.9	Timer for physical deactivation in state F7 Test B	D.3.2.2.5.2	6.2.7		F7/TIF7physdeact
5.10	Timer for complete deactivation in state F7 Test A	D.3.2.2.6.1	6.2.7		F7/TIF7compdeact1
5.11	Timer for complete deactivation in state F7 Test A	D.3.2.2.6.1	6.2.7		F7/TIF7compdeact2
5.12	Timer for complete deactivation in state F8 Test B	D.3.2.2.6.2	6.2.7		F8/TIF8compdeact1
5.13	Timer for complete deactivation in state F8 Test B	D.3.2.2.6.2	6.2.7		F8/TIF8compdeact2

no. 5.10 - 5.13

L2-, L3-protocol for basic call functions according to CTS2-ISDN-Basic Access Appendix B2

1.6 FRAME ALIGNMENT PROCEDURE

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment / Test name
6.1	Frame alignment procedure for one bad frame 96KHz	D.3.3.a	6.3	5.3.a	F7/FAinfA_1fr
6.2	Frame alignment procedure for one bad frame l4noflag	D.3.3.a	6.3	5.3.a	F7/FAinfB_1fr
6.3	Frame alignment procedure for one bad frame l4viol16	D.3.3.a	6.3	5.3.a	F7/FAinfD_1fr
6.4	Frame alignment procedure for n bad frames 96KHz	D.3.3.b	6.3	5.3.b	F7/FAinfA_kfr
6.5	Frame alignment procedure for n bad frames l4noflag	D.3.3.b	6.3	5.3.b	F7/FAinfB_kfr
6.6	Frame alignment procedure for n bad frames l4viol16	D.3.3.b	6.3	5.3.b	F7/FAinfD_kfr
6.7	Frame re-alignment procedure for m good frames	D.3.3.c	6.3	5.3.c	F7/FAregain

1.7 MULTIFRAMING PROCEDURE

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment / Test name
7.1	Multiframing procedure	D.3.4	6.3.3	5.4	F7/MUltiframe

1.8 IDLE CHANNEL CODE

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment / Test name
8.1	Idle channel code on the B-channel	D.3.5	6.4		F7/BCBinaryOne

1.9 FRAME RATE

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
9.1	Bit rate when transmitting INFO1, normal power at 42V	D.4.1	8.1	6.1.1	[AN]
9.2	Bit rate when transmitting INFO1, normal power at 24V	D.4.1	8.1	6.1.1	[AN]
9.3	Bit rate when transmitting INFO1, restricted power at 42V	D.4.1	8.1	6.1.1	[AN]
9.4	Bit rate when transmitting INFO1, restricted power at 32V	D.4.1	8.1	6.1.1	[AN]

1.10 JITTER CHARACTERISTICS

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
10.1	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. I
10.2	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. I
10.3	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. I
10.4	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. I
10.5	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. II
10.6	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. II
10.7	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. II

10.8	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. II
10.9	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. IIIa
10.10	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. IIIa
10.11	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. IIIa
10.12	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1a	[SIM-HC] [JIT]: weighted and spectral config. IIIa
10.13	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1a	[SIM-LHC] [JIT]: weighted and spectral config. IIIb
10.14	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1a	[SIM-LHC] [JIT]: weighted and spectral config. IIIb
10.15	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1a	[SIM-LHC] [JIT]: weighted and spectral config. IIIb
10.16	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1a	[SIM-LHC] [JIT]: weighted and spectral config. IIIb

10.17	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1a	[JIT]: weighted and spectral
10.18	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1a	[JIT]: weighted and spectral
10.19	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1a	[JIT]: weighted and spectral
10.20	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1a	[JIT]: weighted and spectral
10.21	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT]: weighted and spectral config. I
10.22	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT]: weighted and spectral config. I
10.23	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT]: weighted and spectral config. I
10.24	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT]: weighted and spectral config. I
10.25	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2us delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT]: weighted and spectral config. II

10.26	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2us delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT]: weighted and spectral config. II
10.27	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2us delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT]: weighted and spectral config. II
10.28	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2us delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT]: weighted and spectral config. II
10.29	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2us delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT] : weighted and spectral config. IIIa
10.30	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2us delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT] : weighted and spectral config. IIIa
10.31	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2us delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT] : weighted and spectral config. IIIa
10.32	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2us delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1b	[SIM-HC] [JIT] : weighted and spectral config. IIIa

10.33	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continiuous binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1b	[SIM-LHC] [JIT]: weighted and spectral config. IIIb
10.34	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1b	[SIM-LHC] [JIT]: weighted and spectral config. IIIb
10.35	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continiuous binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1b	[SIM-LHC] [JIT]: weighted and spectral config. IIIb
10.36	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1b	[SIM-LHC] [JIT]: weighted and spectral config. IIIb
10.37	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1b	[JIT]: weighted and spectral
10.38	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1b	[JIT]: weighted and spectral
10.39	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1b	[JIT]:weighted and spectral

10.40	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of 40 frames with continuous octets of 0AAH in both B-channels an continuous ones in the D- and D-Echo channels followed by 40 frames with continuous binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1b	[JIT]: weighted and spectral
10.41	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT]: weighted and spectral config. I
10.42	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT]: weighted and spectral config. I
10.43	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT]: weighted and spectral config. I
10.44	Jitter characteristics when transmitting INFO3, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT]: weighted and spectral config. I
10.45	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT]: weighted and spectral config. II
10.46	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT]: weighted and spectral config. II
10.47	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT]: weighted and spectral config. II
10.48	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT]: weighted and spectral config. II
10.49	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT] : weighted and spectral config. IIIa

10.50	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT] : weighted and spectral config. IIIa
10.51	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT] : weighted and spectral config. IIIa
10.52	Jitter characteristics when transmitting INFO3, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1c	[SIM-HC] [JIT] : weighted and spectral config. IIIa
10.53	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.2	6.2.1c	[SIM-LHC] [JIT] : weighted and spectral config. IIIb
10.54	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.2	6.2.1c	[SIM-LHC] [JIT] : weighted and spectral config. IIIb
10.55	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.2	6.2.1c	[SIM-LHC] [JIT] : weighted and spectral config. IIIb
10.56	Jitter characteristics when transmitting INFO3, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.2	6.2.1c	[SIM-LHC] [JIT] : weighted and spectral config. IIIb
10.57	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.1	8.2.3	6.2.1c	[JIT]: weighted and spectral
10.58	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.1	8.2.3	6.2.1c	[JIT]: weighted and spectral

10.59	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.1	8.2.3	6.2.1c	[JIT]: weighted and spectral
10.60	Jitter characteristics when transmitting INFO3, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.1	8.2.3	6.2.1c	[JIT]: weighted and spectral

1.11 INPUT TO OUTPUT OFFSET

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
11.1	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. I
11.2	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. I
11.3	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. I
11.4	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. I
11.5	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. II
11.6	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. II
11.7	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. II
11.8	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. II

11.9	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. IIIa
11.10	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. IIIa
11.11	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. IIIa
11.12	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-HC] config. IIIa
11.13	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-LHC] config. IIIb
11.14	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-LHC] config. IIIb
11.15	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-LHC] config. IIIb
11.16	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2a	[AN][SIM-LHC] config. IIIb
11.17	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN]config. IV
11.18	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2a	[AN]config. IV
11.19	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2a	[AN]config. IV

11.20	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary ones in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2a	[AN]config. IV
11.21	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-HC] config. I
11.22	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-HC] config. I
11.23	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-HC] config. I
11.24	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-HC] config. I
11.25	Input to output offset, short passive bus configuration (low cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-LHC] config. II
11.26	Input to output offset, short passive bus configuration (low cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-LHC] config. II
11.27	Input to output offset, short passive bus configuration (low cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-LHC] config. II
11.28	Input to output offset, short passive bus configuration (low cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-LHC] config. II
11.29	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-HC] config. IIIa

11.30	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-HC] config. IIIa
11.31	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-HC] config. IIIa
11.32	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-HC] config. IIIa
11.33	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-LHC] config. IIIb
11.34	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-LHC] config. IIIb
11.35	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-LHC] config. IIIb
11.36	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2b	[AN][SIM-LHC] config. IIIb
11.37	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN]config. IV
11.38	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2b	[AN]config. IV

11.39	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2b	[AN]config. IV
11.40	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with the octet 0AAH in both B-channels and binary ones in the D- and D-Echo channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2b	[AN]config. IV
11.41	Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3		[AN][SIM-HC] config. I
11.42	Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3		[AN][SIM-HC] config. I
11.43	Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3		[AN][SIM-HC] config. I
11.44	Input to output offset, point to point configuration (high cap. cable with 6 dB attenuation) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3		[AN][SIM-HC] config. I
11.45	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3		[AN][SIM-HC] config. II
11.46	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3		[AN][SIM-HC] config. II
11.47	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3		[AN][SIM-HC] config. II
11.48	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus, with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3		[AN][SIM-HC] config. II
11.49	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3		[AN][SIM-HC] config. IIIa

11.50	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3		[AN][SIM-HC] config. IIIa
11.51	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3		[AN][SIM-HC] config. IIIa
11.52	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3		[AN][SIM-HC] config. IIIa
11.53	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3		[AN][SIM-LHC] config. IIIb
11.54	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3		[AN][SIM-LHC] config. IIIb
11.55	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3		[AN][SIM-LHC] config. IIIb
11.56	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3		[AN][SIM-LHC] config. IIIb
11.57	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3		[AN]config. IV
11.58	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3		[AN]config. IV
11.59	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3		[AN]config. IV
11.60	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with all binary zeroes in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3		[AN]config. IV

11.61	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. I
11.62	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. I
11.63	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. I
11.64	Input to output offset, point to point configuration (high cap. cable with 6dB attenuation) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. I
11.65	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. II
11.66	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. II
11.67	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. II
11.68	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. II
11.69	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. IIIa
11.70	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. IIIa
11.71	Input to output offset, short passive bus configuration (high cap. cable with 2μs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. IIIa

11.72	Input to output offset, short passive bus configuration (high cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-HC] config. IIIa
11.73	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-LHC] config. IIIb
11.74	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-LHC] config. IIIb
11.75	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-LHC] config. IIIb
11.76	Input to output offset, short passive bus configuration (low cap. cable with 2µs delay) with 7 TEs clustered at the far end of the bus, with the UUT-TE adjacent to the signal source, with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2c	[AN][SIM-LHC] config. IIIb
11.77	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN]config. IV
11.78	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, normal power at 24V	D.4.2.2	8.2.3	6.2.2c	[AN]config. IV
11.79	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 42V	D.4.2.2	8.2.3	6.2.2c	[AN]config. IV
11.80	Input to output offset, ideal configuration (direct connection TE to NT) with an input sequence of continuous frames with a 2^{19}-1 PRBS in D, D-Echo and both B channels, restricted power at 32V	D.4.2.2	8.2.3	6.2.2c	[AN]config. IV

1.12 TRANSMITTER OUTPUT IMPEDANCE

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
12.1	Test A: output impedance when transmitting a binary one in state F3, normal power at 42V	D.4.3.1	8.5.1.2 a	6.3.1B	[AN]
12.2	Test A: output impedance when transmitting a binary one in state F3, normal power at 24V	D.4.3.1	8.5.1.2 a	6.3.1B	[AN]
12.3	Test A: output impedance when transmitting a binary one in state F3, restricted power at 42V	D.4.3.1	8.5.1.2 a	6.3.1B	[AN]
12.4	Test A: output impedance when transmitting a binary one in state F3, restricted power at 32V	D.4.3.1	8.5.1.2 a	6.3.1B	[AN]
12.5	Test B: output impedance when transmitting a binary zero, positive pulses into a 50Ω load, normal power at 42V	D.4.3.2	8.5.1.2 b	6.3.2a	[AN] *
12.6	Test B: output impedance when transmitting a binary zero, positive pulses into a 50Ω load, normal power at 24V	D.4.3.2	8.5.1.2 b	6.3.2a	[AN] *
12.7	Test B: output impedance when transmitting a binary zero, positive pulses into a 50Ω load, restricted power at 42V	D.4.3.2	8.5.1.2 b	6.3.2a	[AN] *
12.8	Test B: output impedance when transmitting a binary zero, positive pulses into a 50Ω load, restricted power at 32V	D.4.3.2	8.5.1.2 b	6.3.2a	[AN] *
12.9	Test B: output impedance when transmitting a binary zero, negative pulses into a 50Ω load, normal power at 42V	D.4.3.2	8.5.1.2 b	6.3.2a	[AN] *
12.10	Test B: output impedance when transmitting a binary zero, negative pulses into a 50Ω load, normal power at 24V	D.4.3.2	8.5.1.2 b	6.3.2a	[AN] *
12.11	Test B: output impedance when transmitting a binary zero, negative pulses into a 50Ω load, restricted power at 42V	D.4.3.2	8.5.1.2 b	6.3.2a	[AN] *
12.12	Test B: output impedance when transmitting a binary zero, negative pulses into a 50Ω load, restricted power at 32V	D.4.3.2	8.5.1.2 b	6.3.2a	[AN] *
12.13	Test B: output impedance when transmitting a binary zero, positive pulses into a 400Ω load, normal power at 42V	D.4.3.2	8.5.1.2 b	6.3.2b	[AN] *
12.14	Test B: output impedance when transmitting a binary zero, positive pulses into a 400Ω load, normal power at 24V	D.4.3.2	8.5.1.2 b	6.3.2b	[AN] *
12.15	Test B: output impedance when transmitting a binary zero, positive pulses into a 400Ω load, restricted power at 42V	D.4.3.2	8.5.1.2 b	6.3.2b	[AN] *
12.16	Test B: output impedance when transmitting a binary zero, positive pulses into a 400Ω load, restricted power at 32V	D.4.3.2	8.5.1.2 b	6.3.2b	[AN] *
12.17	Test B: output impedance when transmitting a binary zero, negative pulses into a 400Ω load, normal power at 42V	D.4.3.2	8.5.1.2 b	6.3.2b	[AN] *
12.18	Test B: output impedance when transmitting a binary zero, negative pulses into a 400Ω load, normal power at 24V	D.4.3.2	8.5.1.2 b	6.3.2b	[AN] *

12.19	Test B: output impedance when transmitting a binary zero, negative pulses into a 400Ω load, restricted power at 42V	D.4.3.2	8.5.1.2 b	6.3.2b	[AN] *
12.20	Test B: output impedance when transmitting a binary zero, negative pulses into a 400Ω load, restricted power at 32V	D.4.3.2	8.5.1.2 b	6.3.2b	[AN] *

* double pulses into 50 Ω or 400 Ω (R^+,R^-,R^{+-}) ; isolated pulses (R^+) w. loop

double pulses into 50 Ω or 400Ω (R^+,R^-,R^{+-}) ; isolated pulses (R^-) w. loop

1.13 TRANSMITTER OUTPUT IMPEDANCE

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
12.21	Test C: output peak current when transmitting a binary one in state F3, normal power at 42V	D.4.3.3	8.5.1.2 a	6.3.3	[AN]
12.22	Test C: output peak current when transmitting a binary one in state F3, normal power at 24V	D.4.3.3	8.5.1.2 a	6.3.3	[AN]
12.23	Test C: output peak current when transmitting a binary one in state F3, restricted power at 42V	D.4.3.3	8.5.1.2 a	6.3.3	[AN]
12.24	Test C: output peak current when transmitting a binary one in state F3, restricted power at 32V	D.4.3.3	8.5.1.2 a	6.3.3	[AN]
12.25	Test D: output impedance when transmitting a binary one in state F1	D.4.3.4	8.5.1.2 a	6.3.1A	[AN]
12.26	Test D: output impedance when transmitting a binary one in state F1.0	D.4.3.4	8.5.1.2 a	6.3.4	[AN]
12.27	Test D: output impedance when transmitting a binary one in state F1.1	D.4.3.4	8.5.1.2 a	6.3.1A	[AN]
12.28	Test E: output peak current when transmitting a binary one in state F1	D.4.3.5	8.5.1.2 a	6.3.3	[AN]
12.29	Test E: output peak current when transmitting a binary one in state F1.0	D.4.3.5	8.5.1.2 a	6.3.3	[AN]
12.30	Test E: output peak current when transmitting a binary one in state F1.1	D.4.3.5	8.5.1.2 a	6.3.3	[AN]

1.14 PULSE SHAPE AND AMPLITUDE

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
13.1	Pulse shape and amplitude for positive pulses, normal power at 42V	D.4.4	8.5.3.1	6.4	[AN] note 13a)
13.2	Pulse shape and amplitude for positive pulses, normal power at 24V	D.4.4	8.5.3.1	6.4	[AN] note 13a)
13.3	Pulse shape and amplitude for positive pulses, restricted power at 42V	D.4.4	8.5.3.1	6.4	[AN] note 13a)
13.4	Pulse shape and amplitude for positive pulses, restricted power at 32V	D.4.4	8.5.3.1	6.4	[AN] note 13a)
13.5	Pulse shape and amplitude for negative pulses, normal power at 42V	D.4.4	8.5.3.1	6.4	[AN] note 13a)
13.6	Pulse shape and amplitude for negative pulses, normal power at 24V	D.4.4	8.5.3.1	6.4	[AN] note 13a)
13.7	Pulse shape and amplitude for negative pulses, restricted power at 42V	D.4.4	8.5.3.1	6.4	[AN] note 13a)

13.8	Pulse shape and amplitude for negative pulses, restricted power at 32V	D.4.4	8.5.3.1	6.4	[AN] note 13a)
13.9	Test A: Voltage on a 400Ω load (pulse shape) for positive pulses, normal power at 42V	D.4.6.1	8.5.5.1	6.6.1	[AN] note 13b)
13.10	Test A: Voltage on a 400Ω load (pulse shape) for positive pulses, normal power at 24V	D.4.6.1	8.5.5.1	6.6.1	[AN] note 13b)
13.11	Test A: Voltage on a 400Ω load (pulse shape) for positive pulses, restricted power at 42V	D.4.6.1	8.5.5.1	6.6.1	[AN] note 13b)
13.12	Test A: Voltage on a 400Ω load (pulse shape) for positive pulses, restricted power at 32V	D.4.6.1	8.5.5.1	6.6.1	[AN] note 13b)
13.13	Test A: Voltage on a 400Ω load (pulse shape) for negative pulses, normal power at 42V	D.4.6.1	8.5.5.1	6.6.1	[AN] note 13b)
13.14	Test A: Voltage on a 400Ω load (pulse shape) for negative pulses, normal power at 24V	D.4.6.1	8.5.5.1	6.6.1	[AN] note 13b)
13.16	Test A: Voltage on a 400Ω load (pulse shape) for negative pulses, restricted power at 32V	D.4.6.1	8.5.5.1	6.6.1	[AN] note 13b)
13.17	Test B: Voltage on a 5.6Ω load (pulse shape) for positive pulses, normal power at 42V	D.4.6.2	8.5.5.2	6.6.2	[AN] note 13b)
13.18	Test B: Voltage on a 5.6Ω load (pulse shape) for positive pulses, normal power at 24V	D.4.6.2	8.5.5.2	6.6.2	[AN] note 13b)
13.19	Test B: Voltage on a 5.6Ω load (pulse shape) for positive pulses, restricted power at 42V	D.4.6.2	8.5.5.2	6.6.2	[AN] note 13b)
13.20	Test B: Voltage on a 5.6Ω load (pulse shape) for positive pulses, restricted power at 32V	D.4.6.2	8.5.5.2	6.6.2	[AN] note 13b)
13.21	Test B: Voltage on a 5.6Ω load (pulse shape) for negative pulses, normal power at 42V	D.4.6.2	8.5.5.2	6.6.2	[AN] note 13b)
13.22	Test B: Voltage on a 5.6Ω load (pulse shape) for negative pulses, normal power at 24V	D.4.6.2	8.5.5.2	6.6.2	[AN] note 13b)
13.23	Test B: Voltage on a 5.6Ω load (pulse shape) for negative pulses, restricted power at 42V	D.4.6.2	8.5.5.2	6.6.2	[AN] note 13b)
13.24	Test B: Voltage on a 5.6Ω load (pulse shape) for negative pulses, restricted power at 32V	D.4.6.2	8.5.5.2	6.6.2	[AN] note 13b)

note 13a) Multi Periodic Sampling MPS 12Bit / 24MHz and 1. double pulse 12Bit / 16MHz

5.6 and 400Ω load selectable for double pulse

note 13b) Multi Periodic Sampling MPS 12Bit / 24MHz

1.15 PULSE UNBALANCE

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
14.1	Pulse amplitude, normal power at 42V	D.4.5.1	--		[AN] note 14a)
14.2	Pulse amplitude, normal power at 24V	D.4.5.1	--		[AN] note 14a)
14.3	Pulse amplitude, restricted power at 42V	D.4.5.1	--		[AN] note 14a)
14.4	Pulse amplitude, restricted power at 32V	D.4.5.1	--		[AN] note 14a)
14.5	Pulse unbalance of an isolated couple of pulses, normal power at 42V	D.4.5.2	8.5.4	6.5	[AN] note 14b)

14.6	Pulse unbalance of an isolated couple of pulses, normal power at 24V	D.4.5.2	8.5.4	6.5	[AN] note 14b)
14.7	Pulse unbalance of an isolated couple of pulses, restricted power at 42V	D.4.5.2	8.5.4	6.5	[AN] note 14b)
14.8	Pulse unbalance of an isolated couple of pulses, restricted power at 32V	D.4.5.2	8.5.4	6.5	[AN] note 14b)

note 14a) Multi Periodic Sampling MPS 12Bit / 16MHz

note 14b) Multi Periodic Sampling MPS 12Bit / 16MHz;

digital integration of 1. or 2. double pulse of INFO 3 with binary ones in D- and both B-channels

1.16 LONGITUDINAL CONVERSION LOSS

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
15.1	Transmitter output longitudinal conversion loss in state F3, normal power at 42V	D.4.7a	8.5.6.1	6.7.1a	[AN]
15.2	Transmitter output longitudinal conversion loss in state F3, normal power at 24V	D.4.7a	8.5.6.1	6.7.1a	[AN]
15.3	Transmitter output longitudinal conversion loss in state F3, restricted power at 42V	D.4.7a	8.5.6.1	6.7.1a	[AN]
15.4	Transmitter output longitudinal conversion loss in state F3, restricted power at 32V	D.4.7a	8.5.6.1	6.7.1a	[AN]
15.5	Transmitter output longitudinal conversion loss in state F1	D.4.7b	8.5.6.1	6.7.1b	[AN]

1.17 RECEIVER INPUT CHARACTERISTICS

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
16.1	Test A: Receiver input impedance in state F3, normal power at 42V	D.4.8.1.1	8.6.1.1	6.8.1.1B	[AN]
16.2	Test A: Receiver input impedance in state F3, normal power at 24V	D.4.8.1.1	8.6.1.1	6.8.1B	[AN]
16.3	Test A: Receiver input impedance in state F3, restricted power at 42V	D.4.8.1.1	8.6.1.1	6.8.1B	[AN]
16.4	Test A: Receiver input impedance in state F3, restricted power at 32V	D.4.8.1.1	8.6.1.1	6.8.1B	[AN]
16.5	Test B: Receiver input impedance with an overvoltage (peak current) in state F3, normal power at 42V	D.4.8.1.2	8.6.1.1	6.8.1.2	[AN]
16.6	Test B: Receiver input impedance with an overvoltage (peak current) in state F3, normal power at 24V	D.4.8.1.2	8.6.1.1	6.8.1.2	[AN]
16.7	Test B: Receiver input impedance with an overvoltage (peak current) in state F3, restricted power at 42V	D.4.8.1.2	8.6.1.1	6.8.1.2	[AN]
16.8	Test B: Receiver input impedance with an overvoltage (peak current) in state F3, restricted power at 32V	D.4.8.1.2	8.6.1.1	6.8.1.2	[AN]
16.9	Test C: Receiver input impedance in state F1	D.4.8.1.3	8.6.1.1	6.8.1.1A	[AN]
16.10	Test C: Receiver input impedance in state F1.0	D.4.8.1.3	8.6.1.1	6.8.1.3	[AN]
16.11	Test C: Receiver input impedance in state F1.1	D.4.8.1.3	8.6.1.1	6.8.1.1A	[AN]
16.12	Test D: Receiver input impedance with an overvoltage (peak current) in state F1	D.4.8.1.4	8.6.1.1	6.8.1.2	[AN]

16.13	Test D: Receiver input impedance with an overvoltage (peak current) in state F1.0	D.4.8.1.4	8.6.1.1	6.8.1.2	[AN]
16.14	Test D: Receiver input impedance with an overvoltage (peak current) in state F1.1	D.4.8.1.4	8.6.1.1	6.8.1.2	[AN]

1.18 RECEIVER SENSITIVITY

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
17.1	Receiver sensitivity with 200kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, normal power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. I
17.2	Receiver sensitivity with 200kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, normal power at 24V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. I
17.3	Receiver sensitivity with 200kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. I
17.4	Receiver sensitivity with 200kHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. I
17.5	Receiver sensitivity with 2MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, normal power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. I
17.6	Receiver sensitivity with 2MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, normal power at 24V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. I
17.7	Receiver sensitivity with 2MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. I
17.8	Receiver sensitivity with 2MHz sine wave noise and jitter, short point to point configuration (high cap. cable with 6dB attenuation) with a with a 1.5dB attenuated signal source, restricted power at 32V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. I
17.9	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, normal power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. II
17.10	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, normal power at 24V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. II
17.11	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2μs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. II

17.12	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB attenuated signal source, restricted power at 32V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. II
17.13	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, normal power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. II
17.14	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, normal power at 24V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. II
17.15	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. II
17.16	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 8 TEs (including the UUT-TE) clustered at the far end of the bus with a 1.5dB gain signal source, restricted power at 32V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. II
17.17	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, normal power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. IIIa
17.18	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, normal power at 24V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. IIIa
17.19	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, restricted power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. IIIa
17.20	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, restricted power at 32V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. IIIa
17.21	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, normal power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. IIIa
17.22	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, normal power at 24V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. IIIa
17.23	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, restricted power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. IIIa

17.24	Receiver sensitivity with jitter, short passive bus configuration (high cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, restricted power at 32V	D.4.8.2	8.6.2.1	6.8.2	[SIM-HC] [JIT] : with integrated jitter generator config. IIIa
17.25	Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, normal power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-LHC] [JIT]: with integrated jitter generator config. IIIb
17.26	Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, normal power at 24V	D.4.8.2	8.6.2.1	6.8.2	[SIM-LHC] [JIT]: with integrated jitter generator config. IIIb
17.27	Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, restricted power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-LHC] [JIT]: with integrated jitter generator config. IIIb
17.28	Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB attenuated signal source, restricted power at 32V	D.4.8.2	8.6.2.1	6.8.2	[SIM-LHC] [JIT]: with integrated jitter generator config. IIIb
17.29	Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, normal power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-LHC] [JIT]: with integrated jitter generator config. IIIb
17.30	Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, normal power at 24V	D.4.8.2	8.6.2.1	6.8.2	[SIM-LHC] [JIT]: with integrated jitter generator config. IIIb
17.31	Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, restricted power at 42V	D.4.8.2	8.6.2.1	6.8.2	[SIM-LHC] [JIT]: with integrated jitter generator config. IIIb
17.32	Receiver sensitivity with jitter, short passive bus configuration (low cap. cable with 2µs delay) with 7TEs clustered at the far end of the bus, and the UUT-TE adjacent to the signal source with a 1.5dB gain signal source, restricted power at 32V	D.4.8.2	8.6.2.1	6.8.2	[SIM-LHC] [JIT]: with integrated jitter generator config. IIIb
17.33	Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5dB gain signal source, normal power at 42V	D.4.8.2	8.6.2.1	6.8.2	[JIT] : with integrated jitter generator config. IV
17.34	Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5dB gain signal source, normal power at 24V	D.4.8.2	8.6.2.1	6.8.2	[JIT] : with integrated jitter generator config. IV
17.35	Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5dB gain signal source, restricted power at 42V	D.4.8.2	8.6.2.1	6.8.2	[JIT] : with integrated jitter generator config. IV

17.36	Receiver sensitivity with jitter, ideal configuration (direct connection UUT-TE to NT) with a 1.5dB gain signal source, restricted power at 32V	D.4.8.2	8.6.2.1	6.8.2	[JIT] : with integrated jitter generator config. IV

{#} no. 17.1 - 17.36

jitter amplitude and frequency are defined by ETSI

1.19 RECEIVER UNBALANCE ABOUT EARTH

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
18.1	Receiver unbalance about earth (longitudinal conversion loss) in state F3, normal power at 42V	D.4.8.3a	8.6.4	6.8.3a	[AN]
18.2	Receiver unbalance about earth (longitudinal conversion loss) in state F3, normal power at 24V	D.4.8.3a	8.6.4	6.8.3a	[AN]
18.3	Receiver unbalance about earth (longitudinal conversion loss) in state F3, restricted power at 42V	D.4.8.3a	8.6.4	6.8.3a	[AN]
18.4	Receiver unbalance about earth (longitudinal conversion loss) in state F3, restricted power at 32V	D.4.8.3a	8.6.4	6.8.3a	[AN]
18.5	Receiver unbalance about earth (longitudinal conversion loss) in state F1	D.4.8.3b	8.6.4	6.8.3b	[AN]

1.20 POWER FEEDING

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
19.1	TE consumption from power source 1 in normal mode at 42 VDC in state F7 with an active connection	D.5.1.1.1	9.3.1.1	7.1.1	
19.1a	TE consumption from power source 1 in normal mode at 42 VDC in state F7	D.5.1.1.1	9.3.1.1	7.1.1	
19.2	TE consumption from power source 1 in normal mode at 32 VDC in state F7 with an active connection	D.5.1.1.1	9.3.1.1	7.1.1	
19.2a	TE consumption from power source 1 in normal mode at 32 VDC in state F7	D.5.1.1.1	9.3.1.1	7.1.1	
19.3	TE consumption from power source 1 in normal mode at 24 VDC in state F7 with an active connection	D.5.1.1.1	9.3.1.1	7.1.1	
19.3a	TE consumption from power source 1 in normal mode at 24 VDC in state F7	D.5.1.1.1	9.3.1.1	7.1.1	
19.4	TE consumption from power source 1 in normal mode at 42 VDC in state F3	D.5.1.1.2	9.3.1.1	7.1.2	
19.5	TE consumption from power source 1 in normal mode at 32 VDC in state F3	D.5.1.1.2	9.3.1.1	7.1.2	
19.6	TE consumption from power source 1 in normal mode at 24 VDC in state F3	D.5.1.1.2	9.3.1.1	7.1.2	
19.7	TE consumption from power source 1 in normal mode at 42 VDC in state F3 with local action	D.5.1.1.3	9.3.1.1	7.1.2	
19.8	TE consumption from power source 1 in normal mode at 32 VDC in state F3 with local action	D.5.1.1.3	9.3.1.1	7.1.2	
19.9	TE consumption from power source 1 in normal mode at 24 VDC in state F3 with local action	D.5.1.1.3	9.3.1.1	7.1.2	
19.10	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F1.0	D.5.1.1.4	9.5.2.2		

19.11	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F1.0	D.5.1.1.4	9.5.2.2		
19.12	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F1.0	D.5.1.1.4	9.5.2.2		
19.13	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F2		9.5.2.2		
19.14	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F2		9..2.2		
19.15	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F2		9.5.2.2		
19.16	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F3	D.5.1.1.4	9.5.2.2		
19.17	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F3	D.5.1.1.4	9.5.2.2		
19.18	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F3	D.5.1.1.4	9.5.2.2		
19.19	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F4		9.5.2.2		
19.20	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F4		9.5.2.2		
19.21	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F4		9.5.2.2		
19.22	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F5		9.5.2.2		
19.23	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F5		9.5.2.2		
19.24	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F5		9.5.2.2		
19.25	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F6		9.5.2.2		
19.26	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F6		9.5.2.2		
19.27	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F6		9.5.2.2		
19.28	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F7	D.5.1.1.4	9.5.2.2		
19.29	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F7	D.5.1.1.4	9.5.2.2		

19.30	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F7	D.5.1.1.4	9.5.2.2		
19.31	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F3 with local action	D.5.1.1.4	9.5.2.2		
19.32	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F3 with local action	D.5.1.1.4	9.5.2.2		
19.33	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F3 with local action	D.5.1.1.4	9.5.2.2		
19.34	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F7 with an active connection	D.5.1.1.4	9.5.2.2		
19.35	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F7 with an active connection	D.5.1.1.4	9.5.2.2		
19.36	Locally powered TE able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F7 with an active connection	D.5.1.1.4	9.5.2.2		
19.37	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F1	D.5.1.1.5	9.3.1.1		
19.38	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F1	D.5.1.1.5	9.3.1.1		
19.39	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F1	D.5.1.1.5	9.3.1.1		
19.40	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F2		9.3.1.1		
19.41	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F2		9.3.1.1		
19.42	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F2		9.3.1.1		
19.43	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F3	D.5.1.1.5	9.3.1.1		
19.44	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F3	D.5.1.1.5	9.3.1.1		
19.45	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F3	D.5.1.1.5	9.3.1.1		
19.46	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F4		9.3.1.1		
19.47	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F4		9.3.1.1		
19.48	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F4		9.3.1.1		

19.49	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F5		9.3.1.1		
19.50	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F5		9.3.1.1		
19.51	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F5		9.3.1.1		
19.52	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F6		9.3.1.1		
19.53	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F6		9.3.1.1		
19.54	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F6		9.3.1.1		
19.55	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F7	D.5.1.1.5	9.3.1.1		
19.56	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F7	D.5.1.1.5	9.3.1.1		
19.57	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F7	D.5.1.1.5	9.3.1.1		
19.58	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F3 with local action	D.5.1.1.5	9.3.1.1		
19.59	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F3 with local action	D.5.1.1.5	9.3.1.1		
19.60	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F3 with local action	D.5.1.1.5	9.3.1.1		
19.61	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 42 VDC in state F7 with an active connection	D.5.1.1.5	9.3.1.1		
19.62	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 32 VDC in state F7 with an active connection	D.5.1.1.5	9.3.1.1		
19.63	Locally powered TE not able to detect network power, consumption from power source 1 in normal mode at 24 VDC in state F7 with active connection	D.5.1.1.5	9.3.1.1		
19.64	TE consumption from power source 1 in restricted mode at 42 VDC in state F7 with an active connection	D.5.1.2.1	9.3.1.1	7.2.1	
19.64a	TE consumption from power source 1 in restricted mode at 42 VDC in state F7	D.5.1.2.1	9.3.1.1	7.2.1	
19.65	TE consumption from power source 1 in restricted mode at 32 VDC in state F7 with an active connection	D.5.1.2.1	9.3.1.1	7.2.1	
19.65a	TE consumption from power source 1 in restricted mode at 32 VDC in state F7	D.5.1.2.1	9.3.1.1	7.2.1	
19.66	TE consumption from power source 1 for designated TE in restricted mode at 42 VDC in state F3	D.5.1.2.2	9.3.1.2	7.2.2	

19.67	TE consumption from power source 1 for designated TE in restricted mode at 32 VDC in state F3	D.5.1.2.2	9.3.1.2	7.2.2	
19.68	TE consumption from power source 1 for designated TE in restricted mode at 42 VDC in state F3 with local action	D.5.1.2.3	9.3.1.2	7.2.2	
19.69	TE consumption from power source 1 for designated TE in restricted mode at 32 VDC in state F3 with local action	D.5.1.2.3	9.3.1.2	7.2.2	
19.70	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F1.0	D.5.1.2.4	9.3.1.2	7.2.3	
19.71	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F1.0	D.5.1.2.4	9.3.1.2	7.2.3	
19.72	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F2		9.3.1.2	7.2.3	
19.73	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F2		9.3.1.2	7.2.3	
19.74	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F3	D.5.1.2.4	9.3.1.2	7.2.3	
19.75	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F3	D.5.1.2.4	9.3.1.2	7.2.3	
19.76	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F4		9.3.1.2	7.2.3	
19.77	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F4		9.3.1.2	7.2.3	
19.78	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F5		9.3.1.2	7.2.3	
19.79	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F5		9.3.1.2	7.2.3	
19.80	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F6		9.3.1.2	7.2.3	
19.81	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F6		9.3.1.2	7.2.3	
19.82	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F7	D.5.1.2.4	9.3.1.2	7.2.3	
19.83	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F7	D.5.1.2.4	9.3.1.2	7.2.3	
19.84	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F3 with local action	D.5.1.2.4	9.3.1.2	7.2.3	
19.85	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F3 with local action	D.5.1.2.4	9.3.1.2	7.2.3	

19.86	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F7 with an active connection	D.5.1.2.4	9.3.1.2	7.2.3	
19.87	Locally powered TE able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F7 with an active connection	D.5.1.2.4	9.3.1.2	7.2.3	
19.88	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F1	D.5.1.2.5	9.3.1.2	7.2.4	
19.89	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F1	D.5.1.2.5	9.3.1.2	7.2.4	
19.90	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F2		9.3.1.2	7.2.4	
19.91	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F2		9.3.1.2	7.2.4	
19.92	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F3	D.5.1.2.5	9.3.1.2	7.2.4	
19.93	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F3	D.5.1.2.5	9.3.1.2	7.2.4	
19.94	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F4		9.3.1.2	7.2.4	
19.95	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F4		9.3.1.2	7.2.4	
19.96	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F5		9.3.1.2	7.2.4	
19.97	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F5		9.3.1.2	7.2.4	
19.98	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F6		9.3.1.2	7.2.4	
19.99	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F6		9.3.1.2	7.2.4	
19.100	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F7	D.5.1.2.5	9.3.1.2	7.2.4	
19.101	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F7	D.5.1.2.5	9.3.1.2	7.2.4	
19.102	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F3 with local action	D.5.1.2.5	9.3.1.2	7.2.4	
19.103	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F3 with local action	D.5.1.2.5	9.3.1.2	7.2.4	
19.104	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 42 VDC in state F7 with an active connection	D.5.1.2.5	9.3.1.2	7.2.4	

19.105	Locally powered TE not able to detect network power, consumption from power source 1 in restricted mode at 32 VDC in state F7 with an active connection	D.5.1.2.5	9.3.1.2	7.2.4	
19.106	Not designated TE consumption from power source 1 in restricted mode at 42 VDC in state F1	D.5.1.2.6	9.3.1.2		
19.107	Not designated TE consumption from power source 1 in restricted mode at 32 VDC in state F1	D.5.1.2.6	9.3.1.2		

1.21 CURRENT TRANSIENT

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
20.1a	TE current transient in state F3, normal mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.1b	TE current transient in state F3, normal mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.2a	TE current transient in state F3, normal mode at 32 VDC, positive transient		9.4	7.3.1	
20.2b	TE current transient in state F3, normal mode at 32 VDC, negative transient		9.4	7.3.1	
20.3a	TE current transient in state F3, normal mode at 24 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.3b	TE current transient in state F3, normal mode at 24 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.4a	TE current transient in state F3, restricted mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.4b	TE current transient in state F3, restricted mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.5a	TE current transient in state F3, restricted mode at 32 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.5b	TE current transient in state F3, restricted mode at 32 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.6a	TE current transient in state F4, normal mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.6b	TE current transient in state F4, normal mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.7a	TE current transient in state F4, normal mode at 32 VDC, positive transient		9.4	7.3.1	
20.7b	TE current transient in state F4, normal mode at 32 VDC, negative transient		9.4	7.3.1	
20.8a	TE current transient in state F4, normal mode at 24 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.8b	TE current transient in state F4, normal mode at 24 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.9a	TE current transient in state F4, restricted mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.9b	TE current transient in state F4, restricted mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.10a	TE current transient in state F4, restricted mode at 32 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.10b	TE current transient in state F4, restricted mode at 32 VDC, negative transient	D.5.1.3	9.4	7.3.1	

20.11a	TE current transient in state F5, normal mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.11b	TE current transient in state F5, normal mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.12a	TE current transient in state F5, normal mode at 32 VDC, positive transient		9.4	7.3.1	
20.12b	TE current transient in state F5, normal mode at 32 VDC, negative transient		9.4	7.3.1	
20.13a	TE current transient in state F5, normal mode at 24 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.13b	TE current transient in state F5, normal mode at 24 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.14a	TE current transient in state F5, restricted mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.14b	TE current transient in state F5, restricted mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.15a	TE current transient in state F5, restricted mode at 32 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.15b	TE current transient in state F5, restricted mode at 32 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.16a	TE current transient in state F6, normal mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.16b	TE current transient in state F6, normal mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.17a	TE current transient in state F6, normal mode at 32 VDC, positive transient		9.4	7.3.1	
20.17b	TE current transient in state F6, normal mode at 32 VDC, negative transient		9.4	7.3.1	
20.18a	TE current transient in state F6, normal mode at 24 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.18b	TE current transient in state F6, normal mode at 24 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.19a	TE current transient in state F6, restricted mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.19b	TE current transient in state F6, restricted mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.20a	TE current transient in state F6, restricted mode at 32 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.20b	TE current transient in state F6, restricted mode at 32 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.21a	TE current transient in state F7, normal mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.21b	TE current transient in state F7, normal mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.22a	TE current transient in state F7, normal mode at 32 VDC, positive transient		9.4	7.3.1	
20.22b	TE current transient in state F7, normal mode at 32 VDC, negative transient		9.4	7.3.1	
20.23a	TE current transient in state F7, normal mode at 24 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.23b	TE current transient in state F7, normal mode at 24 VDC, negative transient	D.5.1.3	9.4	7.3.1	

20.24a	TE current transient in state F7, restricted mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.24b	TE current transient in state F7, restricted mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.25a	TE current transient in state F7, restricted mode at 32 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.25b	TE current transient in state F7, restricted mode at 32 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.26a	TE current transient in state F8, normal mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.26b	TE current transient in state F8, normal mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.27a	TE current transient in state F8, normal mode at 32 VDC, positive transient		9.4	7.3.1	
20.27b	TE current transient in state F8, normal mode at 32 VDC, negative transient		9.4	7.3.1	
20.28a	TE current transient in state F8, normal mode at 24 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.28b	TE current transient in state F8, normal mode at 24 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.29a	TE current transient in state F8, restricted mode at 42 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.29b	TE current transient in state F8, restricted mode at 42 VDC, negative transient	D.5.1.3	9.4	7.3.1	
20.30a	TE current transient in state F8, restricted mode at 32 VDC, positive transient	D.5.1.3	9.4	7.3.1	
20.30b	TE current transient in state F8, restricted mode at 32 VDC, negative transient	D.5.1.3	9.4	7.3.1	

1.22 LIMITATION ON POWER SINK DURING TRANSIENT CONDITIONS

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
21.1a	Test 1: TE current vs. time, consumption from power source 1 in normal power mode during connection, T=0..25us	D.5.1.4.1	9.7.1		
21.1b	Test 1: TE current vs. time, consumption from power source 1 in normal power mode during connection, T=0..2s	D.5.1.4.1	9.7.1		
21.2a	Test 2: TE current vs. time, consumption from power source 1 in restricted power mode during connection, T=0..25us	D.5.1.4.1	9.7.1		
21.2b	Test 2: TE current vs. time, consumption from power source 1 in restricted power mode during connection, T=0..2s	D.5.1.4.1	9.7.1		
21.3a	Non designated TE with detector or locally powered TE able to detect network power, current vs. time, consumption from power source 1 in restricted power mode during connection, T=0..250us	D.5.1.4.2a	9.7.1		

ignated TE with detector or locally powered to detect network power, current vs. time, ption from power source 1 in restricted power uring connection,	D.5.1.4.2a	9.7.1		
ignated TE without detector or locally po- E not able to detect network power, current consumption from power source 1 in d power mode during connection, T=0..250us	D.5.1.4.2b	9.7.1		
ignated TE without detector or locally po- E not able to detect network power, current consumption from power source 1 in d power mode during connection,	D.5.1.4.2b	9.7.1		
powered TE able to detect network power, ur upon interruption of power source 1, mode in state F4	D.5.1.4.3	9.7.1		
powered TE able to detect network power, ur upon interruption of power source 1, mode in state F6	D.5.1.4.3	9.7.1		
powered TE able to detect network power, ur upon interruption of power source 1, mode in state F7	D.5.1.4.3	9.7.1		
powered TE able to detect network power, ur upon interruption of power source 1, re- mode in state F4	D.5.1.4.3	9.7.1		
powered TE able to detect network power, ur upon interruption of power source 1, re- in state F6	D.5.1.4.3	9.7.1		
powered TE able to detect network power, ur upon interruption of power source 1, re- mode in state F7	D.5.1.4.3	9.7.1		
start-up test after removal of short circuit in power mode, test a	D.5.1.4.4.1	9.7.3.1		
start-up test after removal of short circuit in power mode, test b	D.5.1.4.4.1	9.7.3.1		
start-up test after removal of short circuit in ed power mode, test a	D.5.1.4.4.1	9.7.3.1		
start-up test after removal of short circuit in ed power mode, test b	D.5.1.4.4.1	9.7.3.1		
start-up test at low input voltage	D.5.1.4.4.2	--		
ion against short term interruptions in normal mode in state F7 with active communications	D.5.1.4.5.1	9.7.3.2		
ion against short term interruptions in re- power mode in state F7 with active com- tions	D.5.1.4.5.2	9.7.3.2		
our at the switch over from normal power o restricted power mode in state F7 with active nications	D.5.1.4.6.1	9.7.3.3		
our at the switch over from restricted power o normal power mode in state F7	D.5.1.4.6.2	9.7.3.3		
C unbalance of TE consumption from power 1 in state F3 at 24 VDC	D.5.1.4.7	9.8.1.1		with option DC-unbalance box
C unbalance of TE consumption from power in state F3 at 40 VDC	D.5.1.4.7	9.8.1.1		with option DC-unbalance box

21.20	Output DC unbalance of TE consumption from power source 1 in state F3 at 24 VDC	D.5.1.4.7	9.8.1.1		with option DC-unbalance box
21.21	Output DC unbalance of TE consumption from power source 1 in state F3 at 40 VDC	D.5.1.4.7	9.8.1.1		with option DC-unbalance box
21.22	Effect of DC unbalance on TE input impedance in state F1.0	D.5.1.4.8	9.8.1.2		with option DC-unbalance box
21.23	Effect of DC unbalance on TE input impedance in state F3	7.1.4.8	9.8.1.2		with option DC-unbalance box

1.23 POWER SOURCE 2 - OPTIONAL THIRD PAIR

no.	PURPOSE	CTS-2-ISDN	CCITT I.430	NET3	Comment
22.1	Power source 2-optional third pair, normal power mode at 42 VDC in state F3	D.5.2a	9.3.2.1		with external adapter
22.2	Power source 2-optional third pair, normal power mode at 42 VDC in state F3 with local action	D.5.2a	9.3.2.1		with external adapter
22.3	Power source 2-optional third pair, normal power mode at 42 VDC in state F7	D.5.2a	9.3.2.1		with external adapter
22.4	Power source 2-optional third pair, normal power mode at 42 VDC in state F7 with an active connection	D.5.2a	9.3.2.1		with external adapter
22.5	Power source 2-optional third pair, normal power mode at 32 VDC in state F3	D.5.2a	9.3.2.1		with external adapter
22.6	Power source 2-optional third pair, normal power mode at 32 VDC in state F3 with local action	D.5.2a	9.3.2.1		with external adapter
22.7	Power source 2-optional third pair, normal power mode at 32 VDC in state F7	D.5.2a	9.3.2.1		with external adapter
22.8	Power source 2-optional third pair, normal power mode at 32 VDC in state F7 with an active connection	D.5.2a	9.3.2.1		with external adapter
22.9	Power source 2-optional third pair, restricted power mode at 42 VDC in state F3	D.5.2b	9.3.2.2		with external adapter
22.10	Power source 2-optional third pair, restricted power mode at 42 VDC in state F3 with local action	D.5.2b	9.3.2.2		with external adapter
22.11	Power source 2-optional third pair, restricted power mode at 42 VDC in state F7	D.5.2b	9.3.2.2		with external adapter
22.12	Power source 2-optional third pair, restricted power mode at 42 VDC in state F7 with an active connection	D.5.2b	9.3.2.2		with external adapter
22.13	Power source 2-optional third pair, restricted power mode at 32 VDC in state F3	D.5.2b	9.3.2.2		with external adapter
22.14	Power source 2-optional third pair, restricted power mode at 32 VDC in state F3 with local action	D.5.2b	9.3.2.2		with external adapter
22.15	Power source 2-optional third pair, restricted power mode at 32 VDC in state F7	D.5.2b	9.3.2.2		with external adapter
22.16	Power source 2-optional third pair, restricted power mode at 32 VDC in state F7 with an active connection	D.5.2b	9.3.2.2		with external adapter

2 TESTS ON NT

2.1 BINARY ORGANISATION OF FRAME

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
11	Binary organisation of INFO4 frames, B1&B2 channels filled with binary 1	--	5.4.2.2	
12	Binary organisation of INFO4 frames, B1&B2 channels filled with 2^9-1 PRBS	E.2.1.1	5.4.2.2	
13	Binary organisation of INFO2 frames	E.2.1.2	6.2.2	

2.2 D CHANNEL ACCESS CONTROL PROCEDURE

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
14	Inter frame (layer 2) time fill of the D channel from the NT	E.3.1	6.1.1	no test specification available; for study
15	D-echo channel response	E.3.2	6.1.5	no test specification available; for study

2.3 ACTIVATION / DEACTIVATION PROCEDURE

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
16	Act.-/Deactivation procedure when receiving PH-AT in state G1	E.3.3.1(1)	6.2	no test specification available; for study
17	Act.-/Deactivation procedure when T1 expires in state G1	E.3.3.1(2)	6.2	no test specification available; for study
18	Act.-/Deactivation procedure when T2 expires in state G1	E.3.3.1(3)	6.2	no test specification available; for study
19	Act.-/Deactivation procedure when receiving INFO0 in state G1	E.3.3.1(4)	6.2	no test specification available; for study
20	Act.-/Deactivation procedure when receiving INFO1 in state G1	E.3.3.1(5)	6.2	no test specification available; for study
21	Act.-/Deactivation procedure when receiving MPH-DR in state G2	E.3.3.1(6)	6.2	no test specification available; for study
22	Act.-/Deactivation procedure when T1 expires in state G2	E.3.3.1(7)	6.2	no test specification available; for study
23	Act.-/Deactivation procedure when T2 expires in state G2	E.3.3.1(8)	6.2	no test specification available; for study
24	Act.-/Deactivation procedure when receiving INFO0 in state G2	E.3.3.1(9)	6.2	no test specification available; for study
25	Act.-/Deactivation procedure when receiving INFO1 in state G2	E.3.3.1(10)	6.2	no test specification available; for study
26	Act.-/Deactivation procedure when receiving INFO3 in state G2	E.3.3.1(11)	6.2	no test specification available; for study
27	Act.-/Deactivation procedure when receiving MPH-DR in state G3	E.3.3.1(12)	6.2	no test specification available; for study
28	Act.-/Deactivation procedure when T2 expires in state G3	E.3.3.1(13)	6.2	no test specification available; for study

29	Act.-/Deactivation procedure when receiving INFO0 in state G3	E.3.3.1(14)	6.2	no test specification available; for study
30	Act.-/Deactivation procedure when receiving INFO3 in state G3	E.3.3.1(15)	6.2	no test specification available; for study
31	Act.-/Deactivation procedure when framing is lost in state G3	E.3.3.1(16)	6.2	no test specification available; for study
32	Act.-/Deactivation procedure when receiving PH-AR in state G4	E.3.3.1(17)	6.2	no test specification available; for study
33	Act.-/Deactivation procedure when T1 expires in state G4	E.3.3.1(18)	6.2	no test specification available; for study
34	Act.-/Deactivation procedure when T2 expires in state G4	E.3.3.1(19)	6.2	no test specification available; for study
35	Act.-/Deactivation procedure when receiving INFO0 in state G4	E.3.3.1(20)	6.2	no test specification available; for study
36	Act.-/Deactivation procedure when receiving INFO1 in state G4	E.3.3.1(21)	6.2	no test specification available; for study
37	Act.-/Deactivation procedure when receiving INFO3 in state G4	E.3.3.1(22)	6.2	no test specification available; for study
38	Act.-/Deactivation procedure when framing is lost in state G4	E.3.3.1(23)	6.2	no test specification available; for study

2.4 TIMERS FOR ACTIVATION / DEACTIVATION

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
39	Activation of timer between the receipt of INFO1 and the transmission of INFO2	E.3.3.2.1a	6.2.6.2	no test specification available; for study
40	Activation of timer between the receipt of INFO3 and the transmission of INFO4	E.3.3.2.1b	6.2.6.2	no test specification available; for study
41	Deactivation of timer between the receipt of INFO0 and the transmission of INFO2	E.3.3.2.2	6.2.7	no test specification available; for study
42	Activation of timer T2	E.3.3.2.3	6.2.7	no test specification available; for study

2.5 FRAME ALIGNMENT PROCEDURE

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
43	Frame alignment procedure for one bad frame	E.3.4a	6.3	no test specification available; for study
44	Frame alignment procedure for n(n>=2) bad frames	E.3.4b	6.3	no test specification available; for study
45	Frame re-alignment procedure for m(m>=3) good frames	E.3.4c	6.3	no test specification available; for study

2.6 JITTER CHARACTERISTICS

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
49	Jitter characteristics when transmitting INFO4, ideal configuration (direct connection NT to signal source) with an output sequence of continuous frames with all binary ones in D and both B channels	E.4.2	8.3	[JIT]: weighted and spectral Basic unit: peak to peak {#}
50	Jitter characteristics when transmitting INFO4, ideal configuration (direct connection NT to signal source) with an output sequence of continuous frames with a $(2^{19}-1)$-PRBS in D and both B channels	E.4.2	8.3	[JIT]: weighted and spectral Basic unit: peak to peak {#}

{#} Activation of the UUT-U_{k0}-interface is required

2.7 TRANSMITTER OUTPUT IMPEDANCE

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
51	Test A: output impedance when transmitting a binary one in state G1 with a 1W power sink on power source 1 in normal mode	E.4.3.1a	8.5.1.1a	[AN] ext. load necessary
52	Test A: output impedance when transmitting a binary one in state G1 with a 420mW power sink on power source 1 in restricted mode	E.4.3.1b	8.5.1.1a	[AN] ext. load necessary
53	Test B: output impedance when transmitting a binary zero, positive pulses into a 50Ω load with a 1W power sink on power source 1 in normal mode	E.4.3.2a	8.5.1.1b	[AN] ext. load necessary
54	Test B: output impedance when transmitting a binary zero, negative pulses into a 50Ω load with a 1W power sink on power source 1 in normal mode	E.4.3.2a	8.5.1.1b	[AN] ext. load necessary
55	Test B: output impedance when transmitting a binary zero, positive pulses into a 50Ω load with a 420mW power sink on power source 1 in restricted mode	E.4.3.2b	8.5.1.1b	[AN] ext. load necessary
56	Test B: output impedance when transmitting a binary zero, positive pulses into a 50Ω load with a 420mW power sink on power source 1 in restricted mode	E.4.3.2b	8.5.1.1b	[AN] ext. load necessary

2.8 PULSE SHAPE AND AMPLITUDE

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
57	Pulse shape and amplitude for positive pulses	E.4.4	8.5.3.1	[AN] *
58	Pulse shape and amplitude for negative pulses	E.4.4	8.5.3.1	[AN] *

* Multi Periodic Sampling MPS 12Bit / 24MHz

2.9 PULSE UNBALANCE

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
59	Pulse amplitude	E.4.5.1	8.5.3.2	not implementable
60	Pulse unbalance of an isolated couple of pulses	E.4.5.2	8.5.4	not implementable

2.10 LONGITUDINAL CONVERSION LOSS

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
61	Transmitter output longitudinal conversion loss in state G1	E.4.6	8.5.6.1	

2.11 RECEIVER INPUT CHARACTERISTICS

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
63	Test A: Receiver input impedance in state G1 with a 1W power sink on power source 1 in normal mode	E.4.7.1.1a	8.6.1.2i	[AN] ext. load necessary
64	Test A: Receiver input impedance in state G1 with a 420mW power sink on power source 1 in restricted mode	E.4.7.1.1b	8.6.1.2i	[AN] ext. load necessary
65	Test B: Receiver input impedance with an overvoltage (peak current) in state G1 with a 1W power sink on power source 1 in normal mode	E.4.7.1.2a	8.6.1.2ii	[AN] ext. load necessary
66	Test B: Receiver input impedance with an overvoltage (peak current) in state G1 with a 420mW power sink on power source 1 in restricted mode	E.4.7.1.2b	8.6.1.2ii	[AN] ext. load necessary

2.12 RECEIVER SENSITIVITY

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
67	Receiver sensitivity without noise or jitter, short passive bus configuration (high cap. cable with 1μs delay) with 8TEs (including the signal source) clustered at the far end of the bus with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.2	[SIM-HC]
68	Receiver sensitivity without noise or jitter, short passive bus configuration (high cap. cable with 1μs delay) with 8TEs (including the signal source) clustered at the far end of the bus with a 1.5dB gain signal source	E.4.7.2	8.6.2.2	[SIM-HC]
69	Receiver sensitivity without noise or jitter, short passive bus configuration (low cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.2	[SIM-LHC]
70	Receiver sensitivity without noise or jitter, short passive bus configuration (low cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB gain signal source	E.4.7.2	8.6.2.2	[SIM-LHC]

71	Receiver sensitivity without noise or jitter, short passive bus configuration (high cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.2	[SIM-HC]
72	Receiver sensitivity without noise or jitter, short passive bus configuration (high cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB gain signal source	E.4.7.2	8.6.2.2	[SIM-HC]
73	Receiver sensitivity with 200kHz sine wave noise and jitter, point to point configuration (high cap. cable with 6dB attenuation) with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.3 8.6.2.5	[SIM-HC] [JIT]
74	Receiver sensitivity with 2MHz sine wave noise and jitter, point to point configuration (high cap. cable with 6dB attenuation) with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.3 8.6.2.5	[SIM-HC] [JIT]
75	Receiver sensitivity with 200kHz sine wave noise and jitter, short passive bus configuration (high cap. cable with 1μs delay) with 8TEs (including the signal source) clustered at the far end of the bus with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.3	[SIM-HC] [JIT]
76	Receiver sensitivity with 200kHz sine wave noise and jitter, short passive bus configuration (high cap. cable with 1μs delay) with 8TEs (including the signal source) clustered at the far end of the bus with a 1.5dB gain signal source	E.4.7.2	8.6.2.3	[SIM-HC] [JIT]
77	Receiver sensitivity with 2MHz sine wave noise and jitter, short passive bus configuration (high cap. cable with 1μs delay) with 8TEs (including the signal source) clustered at the far end of the bus with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.3	[SIM-HC] [JIT]
78	Receiver sensitivity with 2MHz sine wave noise and jitter, short passive bus configuration (high cap. cable with 1μs delay) with 8TEs (including the signal source) clustered at the far end of the bus with a 1.5dB gain signal source	E.4.7.2	8.6.2.3	[SIM-HC] [JIT]
79	Receiver sensitivity with 200kHz sine wave noise and jitter, short passive bus configuration (low cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.3	[SIM-LHC] [JIT]
80	Receiver sensitivity with 200kHz sine wave noise and jitter, short passive bus configuration (low cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB gain signal source	E.4.7.2	8.6.2.3	[SIM-LHC] [JIT]
81	Receiver sensitivity with 200kHz sine wave noise and jitter, short passive bus configuration (high cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.3	[SIM-HC] [JIT]
82	Receiver sensitivity with 200kHz sine wave noise and jitter, short passive bus configuration (high cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB gain signal source	E.4.7.2	8.6.2.3	[SIM-HC] [JIT]

83	Receiver sensitivity with 2MHz sine wave noise and jitter, short passive bus configuration (low cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.3	[SIM-LHC] [JIT]
84	Receiver sensitivity with 2MHz sine wave noise and jitter, short passive bus configuration (low cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB gain signal source	E.4.7.2	8.6.2.3	[SIM-LHC] [JIT]
85	Receiver sensitivity with 2MHz sine wave noise and jitter, short passive bus configuration (high cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.3	[SIM-HC] [JIT]
86	Receiver sensitivity with 2MHz sine wave noise and jitter, short passive bus configuration (high cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus, and the UUT-NT adjacent to the signal source with a 1.5dB gain signal source	E.4.7.2	8.6.2.3	[SIM-HC] [JIT]
87	Receiver sensitivity with 200kHz sine wave noise and jitter, ideal configuration (direct connection UUT-NT to signal source) with a 1.5dB gain signal source	E.4.7.2	8.6.2.3 8.6.2.5	[JIT]
88	Receiver sensitivity with 2MHz sine wave noise and jitter, ideal configuration (direct connection UUT-NT to signal source) with a 1.5dB gain signal source	E.4.7.2	8.6.2.3 8.6.2.5	[JIT]
89	Receiver sensitivity with 200kHz sine wave noise without jitter, ideal configuration (direct connection UUT-NT to signal source) with a 1.5dB gain signal source	E.4.7.2	8.6.2.4	
90	Receiver sensitivity with 2MHz sine wave noise without jitter, ideal configuration (direct connection UUT-NT to signal source) with a 1.5dB gain signal source	E.4.7.2	8.6.2.4	
91	Receiver sensitivity with 200kHz sine wave noise without jitter, extended passive bus configuration with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.4	
92	Receiver sensitivity with 2MHz sine wave noise without jitter, extended passive bus configuration (high cap. cable with 3.8dB loss) with 4TEs (including the signal source) connected giving a 1μs differential delay with a 1.5dB attenuated signal source	E.4.7.2	8.6.2.4	[SIM-HC]

2.13 RECEIVER INPUT DELAY

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
93	Receiver input delay, short passive bus configuration (high cap. cable with 1μs delay) with 8TEs (including the signal source) clustered at the far end of the bus	E.4.7.3	8.6.3.1	[SIM-HC]
94	Receiver input delay, short passive bus configuration (low cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus and the UUT-NT adjacent to the signal source	E.4.7.3	8.6.3.1	[SIM-LHC]
95	Receiver input delay, short passive bus configuration (high cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus and the UUT-NT adjacent to the signal source	E.4.7.3	8.6.3.1	[SIM-HC]
96	Receiver input delay, point to point configuration (high cap. cable with 6dB attenuation)	E.4.7.3	8.6.3.2	[SIM-HC]
97	Receiver input delay, short passive bus configuration (high cap. cable with 1μs delay) with 8TEs (including the signal source) clustered at the far end of the bus	E.4.7.3	8.6.3.2	[SIM-HC]
98	Receiver input delay, short passive bus configuration (low cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus and the UUT-NT adjacent to the signal source	E.4.7.3	8.6.3.2	[SIM-LHC]
99	Receiver input delay, short passive bus configuration (high cap. cable with 1μs delay) with 7TEs clustered at the far end of the bus and the UUT-NT adjacent to the signal source	E.4.7.3	8.6.3.2	[SIM-HC]
100	Receiver input delay , extended passive bus configuration (high cap. cable with 3.8dB loss) with 4TEs (including the signal source) connected giving a 1μs differential delay	E.4.7.3	8.6.3.3	[SIM-HC]
101	Receiver input delay, point to point configuration (high cap. cable with 6dB attenuation).	E.4.7.3	8.6.3.4	[SIM-HC]

{#} no.93...↑01

counting of bit errors for 1 minute; for that a B-channel test loop on LT is required (e.g. with NT-analyzer K1400)

2.14 RECEIVER UNBALANCE ABOUT EARTH

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
102	Receiver unbalance about earth (longitudinal conversion loss) in state G1	E.4.7.4	8.6.4	[AN]
103	Receiver unbalance about earth (longitudinal conversion loss) in state G3	E.4.7.4	8.6.4	[AN]

2.15 POWER FEEDING

no.	PURPOSE	Annex E ETS	CCITT I.430	Comment
104	Maximum power from power source 1 in normal power conditions	E.5.1.1	9	
105	Maximum power source 1 sink in restricted power conditions	E.5.1.2	9	
106	Power source 1 switch over time between normal and restricted power conditions	E.5.1.3	9	
107	Power source 1 switch over time between restricted and normal power conditions	E.5.1.3	9	
108	Restricted mode power source 1 output current under overload conditions (output voltage forced to 1 VDC)	E.5.1.4.1	9	
109	Restricted mode power source 1 output current under overload conditions (output voltage forced to 34 VDC starting from 1 VDC)	E.5.1.4.2	9	
110	Restricted mode power source 1 output current under overload conditions (output voltage forced to 34 VDC starting from nominal load conditions)	E.5.1.4.3	9	
111	Restricted mode power source 1 capability to increase output voltage under capacitive load	E.5.1.4.4	9	
112	Power source 1 in normal power mode recovery from short circuit at minimum input voltage of main supply	E.5.1.5	9	
113	Switch on surge capability of power source 1 in normal mode	E.5.1.6	9	
114	TE connection capability of power source 1 in normal mode	E.5.1.7	9	
115	DC unbalance of power source 1	E.5.1.8	--	not implementable
116	Effect of current unbalance on NT output impedance in state G1	E.5.1.9	--	not implementable
117	Effect of current unbalance on NT input impedance in state G1	E.5.1.9	--	not implementable
118	Minimum output voltage of power source 2	E.5.2	9	

no. 112-113 These tests are also usable for APS-tests (additional power source) E.6.1.3-6.1.5

SIEMENS

ISDN S_0 Analyzer K1403

Jitter

User Manual C73000-B6076-C56-2

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CE

The product described in this manual complies with the statutory regulations on electromagnetic compatibility of devices (EMC) or the regulations of the guideline of the council from 03.05.1989 for adaptation of the statutory regulations of the member countries on electromagnetic compatibility of devices (89/336/EEC).

nts

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1 Safety information

The ISDN S_0 Analyzer K1403 has been constructed and tested in accordance with Publication EN61010, Safety Provisions for Electronic Measuring Equipmentand has left the factory in a perfectly safe condition. In order to maintain optimum safety and ensure hazard-free operation, please adhere to the following basic rules.

- Transport the device only in its original packing or by using the transport case specially recommended for the K1403. This will protect the device against shocks.
- The K1403 is exclusively intended for indoor use. Condensation may occur when the unit is brought to its site of operation from a cold environment. Operation is only permissible with an absolutely dry unit after its temperature has adjusted to the environment.
- Before implementing and operating the K1403, make sure that the environmental conditions are complied with. The environmental conditionsare listed under the heading "Technical data" in the appendix.
- Before switching on the device, make sure that the preset operating voltage of the device corresponds to the permissible line voltage.
- Make sure that replacement fuses are of the specified type and rating: Use: 3.15 A/250V (type T) fuses.
- The power plug must only be inserted into a grounded socket. Do not cancel the protective effect by using an extension cable without a protective ground conductor.
- Make sure that the ventilation slots on the rear and top of the device are not covered.
- The unit can become dangerous if the protective ground conductor is interrupted either inside or outside the unit. Do not interrupt the protective ground conductor intentionally. The same applies when loosening the connection for the protective ground conductor. When opening covers or removing parts, remember that live parts may be exposed if the unit is connected. Connection points may also be live. Disconnect the unit from all voltage sources prior to adjustment, maintenance, repair or when replacing parts. If such work on live and open units cannot be avoided, it should only be performed by qualified staff familiar with the hazard involved.

- All modules contain electro-sensitive components. Please note the necessary precautions and ESD safety measures:

Warning!

When electrical devices are in operation certain parts of these device are live. Non-observance of the above precautions may therefore lead to severe physical injuries or to serious material damage.

Only qualified staff may handle this device or work in its vicinity. They must be thoroughly familiar with all the warnings, safety and maintenance information contained in these instructions. Faultless and safe operation of the device presupposes proper transport, proper storage, set-up and mounting as well as careful handling and servicing.

2 Device description

The jitter module is supplied with three coaxial connection cables (BNC, l =250 mm) and operating manual.

2.1 Jitter

The jitter option enables the jitter or jitter sensitivity of TEs and NTs to be measured together with the K1403 basic unit.

The use of the jitter module thus enables the measurement of jitter parameters as defined in the CCITT I.430 recommendation.

The measurements are carried out in accordance with ETS 300 012 and CTS-2.

Design and Mode of Operation

The plug-in module contains two functional units. One unit contains a phase jitter meter which evaluates the peak and RMS values of the jitter and displays a spectrum of the frequency components (FFT analysis).

The other unit can be used to jitter the magnitude and frequency of the S_0 signal generated by the K1403.

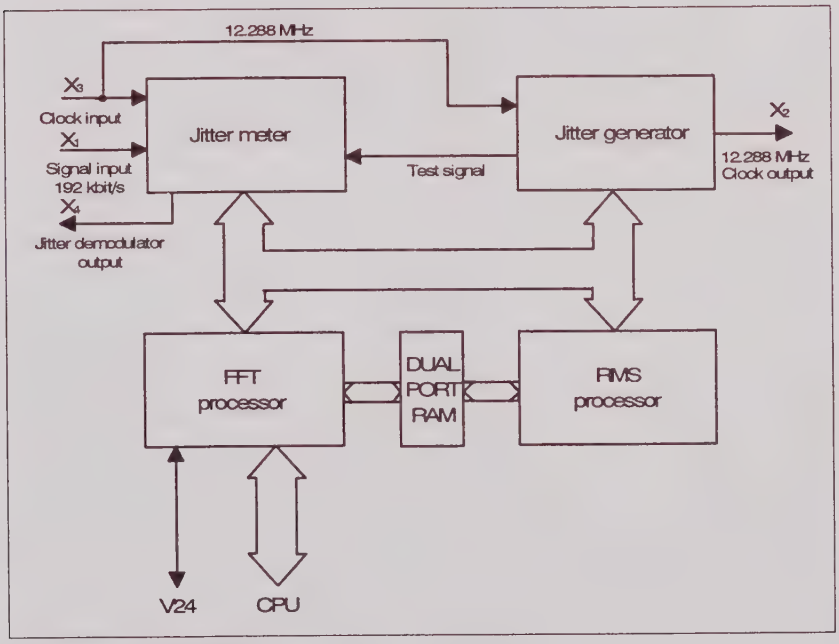


Fig. 2.1: Block diagram

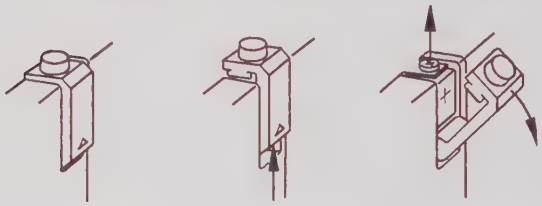
3 Start-up preparations

The following pages will tell you how to make the ISDN S_0 Analyzer ready for use. It will also tell you what you must observe when mounting the K1403 modules.

3.1 Mounting a module

First, remove the cover of the device. The fixing screws for the cover are covered by four corner latches. Proceed as follows:

➤ Push the corner latches some 4 mm upward in direction of the arrow until you meet resistance and unhinge the corner latches.



➤ Loosen the four screws which are now accessible and remove the cover.

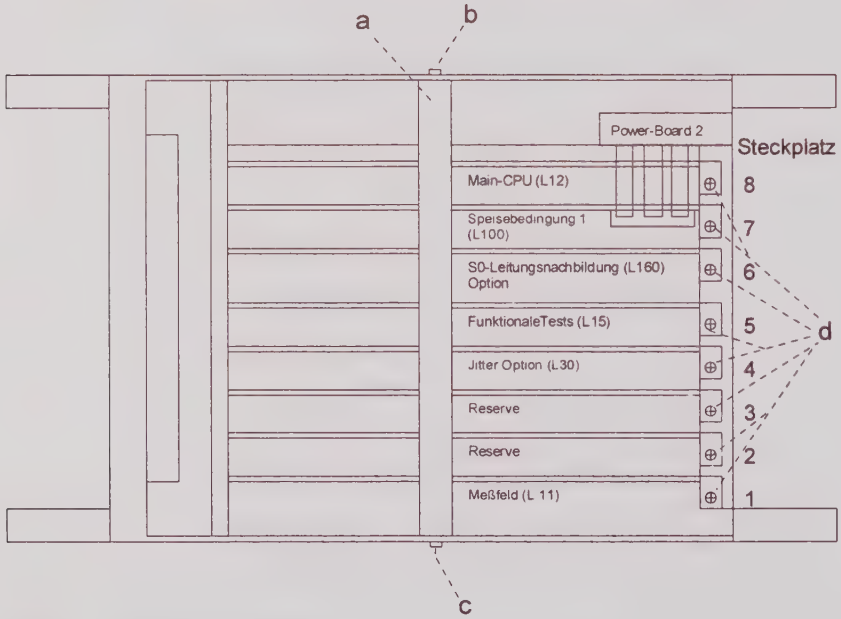


Fig. 3.1: Set-up of the modules

➤ Take the support (a) out by removing screws (b) and (c).

➤ Loosen the module slot screw (d). Insert the module into its destined slot. Ensure that it is correctly assigned and properly fitted in the guide support.

➤ Tighten the module slot screw (d). Re-mount the support (a). Position the printed board in the grooves of the support and tighten screws (b) and (c).

➤ Re-attach the cover of the device.

3.2 Connection of coaxial cables

Four BNC jacks on rear panel

X1 Data input 192 kbit/s

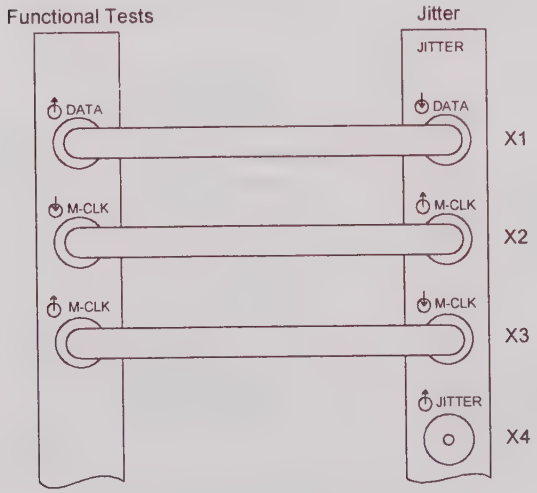
X2 Clock output 12.288 MHz / 15.36 MHz

X3 Clock input 12.288 MHz / 15.36 MHz (system)

X4 Jitter demodulator output

Wiring

Three BNC cables are part of the scope of delivery. These must be connected to the data input X1, clock output X2 and clock input X3 and to the corresponding outputs (data, clock) and the clock input of the module Functional Tests.



4 Operation

The required measuring mode, the test parameters and all equipment parameters are clearly arranged on a large, self-luminous electroluminescent display and set with the aid of operator prompting (menu technique).

Operator prompting is performed with selection windows and interactively changing softkey combinations. Functions or parameters are selected by simply touching the relevant part of the touch screen. No pressure needs to be exerted. Each selection is acknowledged by inversion and is implemented when the panel is exited.

If several setting parameters are offered, these are combined into a single selection window. This window appears after the parameter, e.g. transmitted level has been selected and is deleted after a value has been selected.

There are only two menu levels: the basic menu (which appears after switch-on), and the working menu. The latter is actively adapted, i.e. expanded or simplified, to the given setting or operating mode (START, STOP, RESULT).

Only those touch panels which are necessary or expedient for an application are faded in. Other possibilities need not be taken into account.

4.1 Control elements and sockets

DATA

Signal input

Socket	BNC
Input impedance	> 500 Ω
Input voltage U_{ss}	2 V at 500 Ω
Signal form	192 kbit/s AMI code

M-CLK

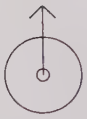
Clock output

Socket	BNC
Output impedance	≤ 4Ω
Output voltage	4 V<U_{ss}< 5 V at R_{out} = 75 Ω
Signal form	12.288 MHz square TE mode
	15.36 MHz square NT mode

M-CLK

Clock input

Socket	BNC
Input impedance	≥3 kΩ
Input voltage U_{ss}	CMOS level / 5V
Signal form	12.288 MHz square TE mode
	15.36 MHz square TE and NT mode

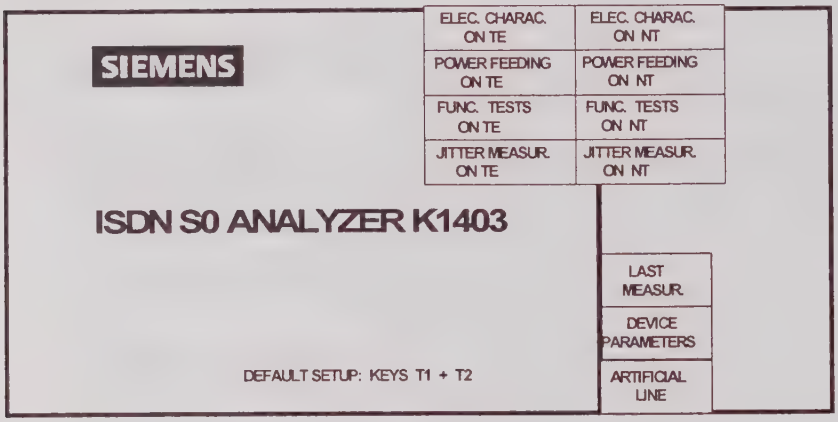


JITTER

Jitter demodulator output

Socket	BNC
Output impedance	< 4 Ω
Output voltage	0 to 5.6 V at 0 to 20% UI_{ss}
	0 to 5.6 V at 0 to 10% UI_{ss}
	0 to 2.8 V at 0 to 5% UI_{ss}

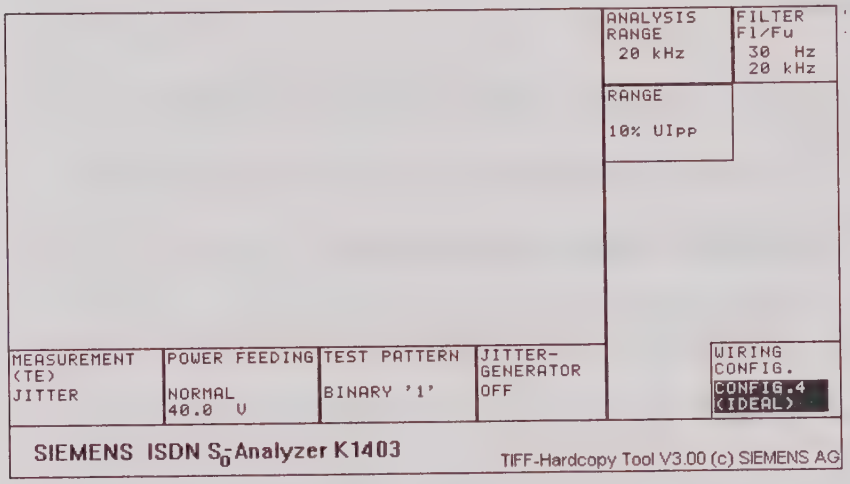
4.2 Summary of operation



5 Measurement and presentation of results

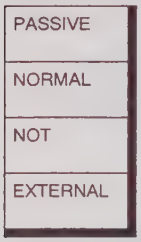
5.1 Jitter measurement TE

If you touch the panel `Jitter Measurement on TE` in the basic menu, a working menu appears for the measurement and creation of phase jitter on TE.


ANALYSIS RANGE 20 kHz
FILTER Fl/Fu 30 Hz 20 kHz
RANGE 10% UIpp
MEASUREMENT (TE) JITTER
POWER FEEDING NORMAL 40.0 V
TEST PATTERN BINARY '1'
JITTER-GENERATOR OFF
WIRING CONFIG. CONFIG.4 (IDEAL)
SIEMENS ISDN S0-Analyzer K1403
TIFF-Hardcopy Tool V3.00 (c) SIEMENS AG

The jitter measurement is optional and can only be carried out if the corresponding module is plugged in.

First, adjust the feeding voltage to the device under test via the panel POWER.



POWER

This panel opens another menu in which the following settings can be selected:

PASSIVE
The device under test is not powered.

Normal
The feeding voltage is applied to the device under test.

NOT
Reverse feeding voltage is applied to the device under test.

The panels NORMAL and NOT open an editing menu.

EDIT
Apart from the preset voltage 40V any desired voltage value between 0V and 56.5V may be set in an editing panel (to be called up via EDIT).

EXTERNAL
The feeding voltage can be routed via sockets U_1 and U_2 at the rear of the device (feeding, slot 7).

The selected feeding voltage will be applied to the S_0 sockets after the START key has been activated.

Other device settings will depend on your particular measurement tasks:

TRANSMISSION FRAME

This panel opens another menu in which the following settings can be selected:

BINARY '1'

Continuous 1 is sent

BINARY '0'

Continuous 0 is sent

ALTERN.FRAME

Transmission signal in acc. with IUT I.430 8.2.2. b)

PRBS 2^9-1

A pseudo random signal 2^9-1 is sent in the channels B1, B2, D and D echo.

PRBS 2^{11}-1

A pseudo random signal 2^{11}-1 is sent in the channels B1, B2, D and D echo.

PRBS 2^{15}-1

A pseudo random signal 2^{15}-1 is sent in the channels B1, B2, D and D echo.

PRBS 2^{19}-1

A pseudo random signal 2^{19}-1 is sent in the channels B1, B2, D and D echo.

EXTERNAL B1

External data can be coupled into the B1 channel via the B-IN socket on the front panel of the device.

EXTERNAL B1+B2

External data can be coupled into the B1+B2 channel via the B-IN socket on the front panel of the device.

ANALYSIS RANGE

For analysis of the power spectrum density you can choose between two frequency ranges: 2 Hz - 20 kHz is preset. The frequency range 10 Hz to 200 Hz is especially intended for analysis of system disturbances.

RANGE

Phase jitter measuring ranges: The following phase jitter measuring ranges can be set: 0 - 5% UI, 0 - 10% UI and 0 - 20% UI.

FILTER FU/FO

This panel opens another menu in which you can select the following settings:

<1 Hz	50 Hz
5 HZ	80 Hz
10 Hz	110 Hz
15 Hz	
30 Hz	next

High pass filters <1 Hz, 5 Hz, 10 Hz, 15 Hz, 30 Hz, 50 Hz, 80 Hz and 110 Hz can be selected (reference: 3 dB limit frequency). Attenuation of the high passes is 20 dB/decade.

You can either select a new frequency limit or confirm the preset high pass via NEXT. Another menu will be opened:

40 Hz	3 kHz
270 HZ	10 kHz
350 Hz	20 kHz
600 Hz	40 kHz
1 kHz	next

Low pass filters 40 Hz, 270 Hz, 350 Hz, 600 Hz, 1 kHz, 3 kHz, 10 kHz, 20 kHz and 40 kHz can be selected (reference: 3 dB limit frequency). Attenuation of the low pass filters is 20 dB/decade.

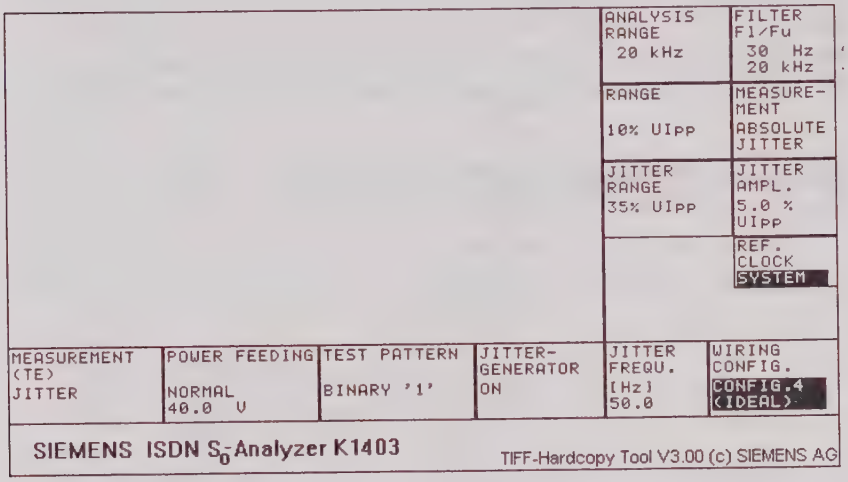
You can either select a new frequency limit or confirm the preset low pass via NEXT.

JITTER GENERATOR

Switching the jitter generator on or off.

JITTER GENERATOR ON

Having switched on the jitter generator you will obtain the following additional setting options:


ANALYSIS RANGE 20 kHz
FILTER F1/Fu 30 Hz 20 kHz
RANGE 10% UIpp
MEASUREMENT ABSOLUTE JITTER
JITTER RANGE 35% UIpp
JITTER AMPL. 5.0 % UIpp
REF. CLOCK SYSTEM
MEASUREMENT (TE) JITTER
POWER FEEDING NORMAL 40.0 V
TEST PATTERN BINARY '1'
JITTER-GENERATOR ON
JITTER FREQU. [Hz] 50.0
WIRING CONFIG. CONFIG.4 (IDEAL)
SIEMENS ISDN S0-Analyzer K1403
TIFF-Hardcopy Tool V3.00 (c) SIEMENS AG

JITTER FREQUENCY

Die Jitterfrequenz kann im frequency range 0.1 Hz - 20 kHz eingestellt werden.

JITTER RANGE

You can choose between the jitter deviation ranges 35% UI and 70% UI.

JITTER DEVIATION

With the EDIT panel, a jitter deviation of 0.4% UI_{ss} to 35% UI_{ss} can be set for the jitter range 35% UI in steps of 0, 2%UI_{ss} and a jitter deviation of 0.8% UI_{ss} to 70% UI_{ss} can be set for the jitter range 70% UI in steps of 0, 4%UI_{ss}.

For the jitter range 35% UI a jitter deviation of 5% UI is set with the panel 5% UI and for the jitter range 70% UI a jitter deviation of 10% UI is set with the panel 10% UI.

ABSOLUTE MEASUREMENT/RELATIVE MEASUREMENT

The following settings are possible:

ABSOLUTE JITTER MEASUREMENT

The measuring signal is demodulated on the basis of a reference signal derived from the unjittered master clock (M-CLK/12.288 MHz). It is displayed in the form of a phase jitter.

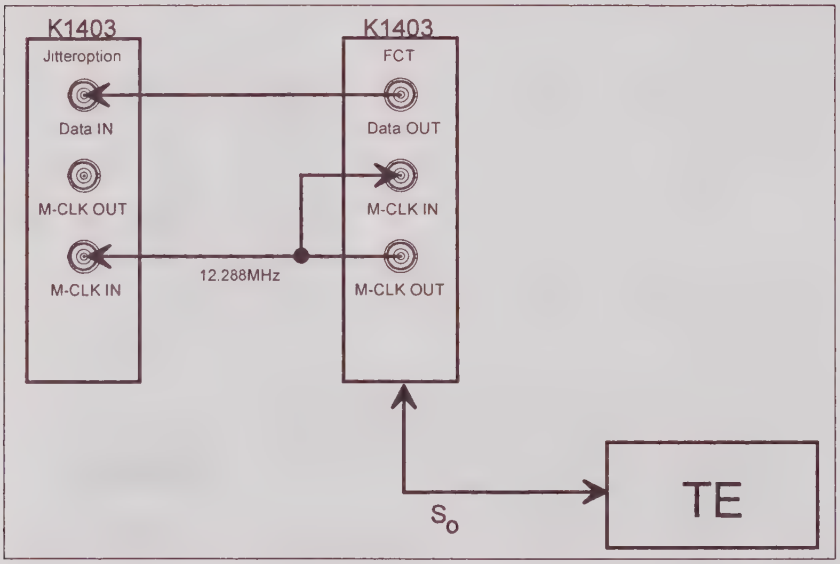
RELATIVE JITTER MEASUREMENT

The measuring signal is demodulated on the basis of a reference signal derived from the jittered master clock (M-CLK/12.288 MHz). It is displayed in the form of a phase jitter.

Measurement set-up

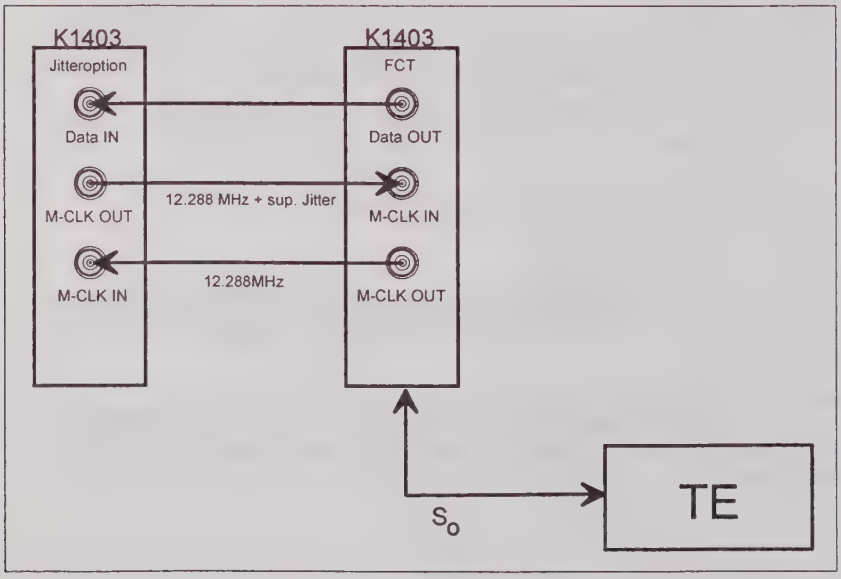
The device under test is connected to the K1403 via Bu 6 or Bu 7.

Jitter measurement with JITTER GENERATOR/OFF:



Jitter measurement with JITTER GENERATOR/ON:

The transmission signal to S_0 is jittered. For that, the 12.288 MHz master clock in the module Option Jitter L30 is superimposed with jitter and is looped back to the module Functional Test L15. A jitter amplitude of 1UI corresponds to a time interval of 5.208333 μs.



Measurement

Start the measurement via the START/STOP key!

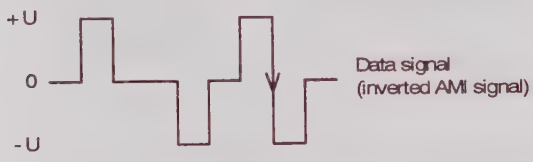
First, the module JITTER is initialized. Then, the following status message "INIT/START" is displayed.

Afterwards, the device under test is activated by way of the U interface module. The activation of the NT necessary for jitter measurement is carried out automatically. Following successful activation the jitter measurement is started. The actual start of the measurement is indicated by "MEASURE".

A complete measuring cycle within the selected frequency range inclusive of all calculations, evaluations and the graphic output on the display takes some 1.3 seconds.

Stop the measurement via the START/STOP key. The status message "STOP" will appear in the display. The device under test is brought to state F3.

The input circuit of the phase jitter meter is configured such that the negative going transition of the data signal from +U to -U is used for jitter evaluation.



If the measurement supplement TM-Box (Toolkit) is connected between the device under test and K1403, the jitter of the increasing or simultaneously the jitter of both edges can be measured additionally.

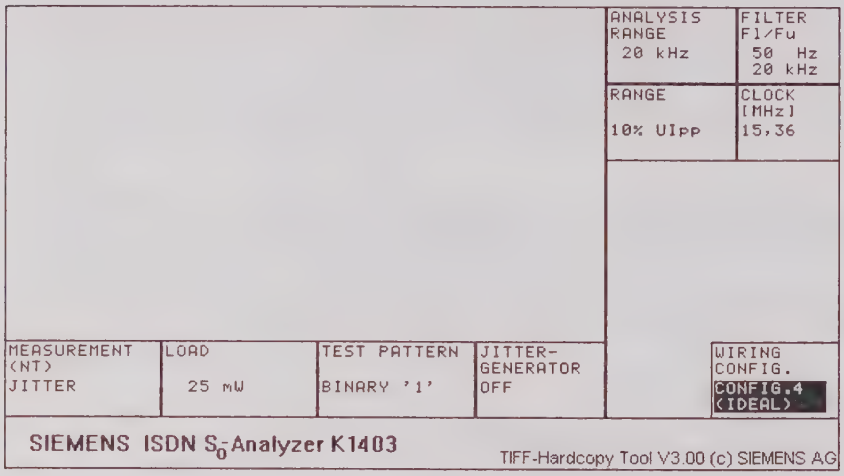
Here, a distinction between absolute and relative jitter measurement is applicable:

- Absolute jitter measurement: The unjittered system clock is used as a reference for establishing the measured values.

- Relative jitter measurement: The jittered transmission signal is used as a reference for establishing the measured values.

5.2 Jitter measurement NT

If you touch the panel `Jitter Measurement on NT` in the basic menu, a working menu appears for the measurement and creation of phase jitter on NT.



The jitter measurement is optional and can only be carried out if the corresponding module is plugged in.

First, adjust the load to the device under test via the panel `LOAD`.

OFF
25 mW
380 mW
1000 mW
EXTERNAL

`Load`

`OFF`
No load is applied to the device under test.

`25MW, 380 MW OR 1000MW`
A load of optionally 25 mW, 380 mW or 1000mW is applied to the device under test.

EXTERNAL
The feeding voltage can be routed via sockets U_1 and U_2 at the rear of the device (module Feeding, slot 7).

The selected load is applied to the S_0 sockets after the START button has been operated.

Other device settings will depend on your particular measurement tasks:

TRANSMISSION FRAME

This panel opens another menu in which the following settings can be selected:

BINARY '1'

Continuous 1 is sent

BINARY '0'

Continuous 0 is sent

ALTERN.FRAME

Transmission signal in acc. with IUT I.430 8.2.2. b)

PRBS 2^9-1

A pseudo random signal 2^9-1 is sent in the channels B1, B2, D and D echo.

PRBS 2^{11}-1

A pseudo random signal 2^{11}-1 is sent in the channels B1, B2, D and D echo.

PRBS 2^{15}-1

A pseudo random signal 2^{15}-1 is sent in the channels B1, B2, D and D echo.

PRBS 2^{19}-1

A pseudo random signal 2^{19}-1 is sent in the channels B1, B2, D and D echo.

EXTERNAL B1

External data can be coupled into the B1 channel via the B-IN socket on the front panel of the device.

EXTERNAL B1+B2

External data can be coupled into the B1+B2 channel via the B-IN socket on the front panel of the device.

ANALYSIS RANGE

For analysis of the power spectrum density you can choose between two frequency ranges: 2 Hz - 20 kHz is preset. The frequency range is especially intended for analysis of system disturbances 10 Hz to 200 Hz.

RANGE

Phase jitter measuring ranges: Folgende The following phase jitter measuring ranges can be set: 0 - 5% UI, 0 - 10% UI and 0 - 20% UI.

CLOCK.

Depending on the measurement set-up, with this panel an input clock of 12.288 Mhz or 15.36 MHz can be selected for the module Option Jitter.

FILTER FU/FO

This panel opens another menu in which you can select the following settings:

<1 Hz	50 Hz
5 HZ	80 Hz
10 Hz	110 Hz
15 Hz	
30 Hz	next

High pass filters <1 Hz, 5 Hz, 10 Hz, 15 Hz, 30 Hz, 50 Hz, 80 Hz and 110 Hz can be selected (reference: 3 dB limit frequency). Attenuation of the high passes is 20 dB/decade.

You can either select a new frequency limit or confirm the preset high pass via NEXT. Another menu will be opened:

	3 kHz
270 HZ	10 kHz
350 Hz	20 kHz
600 Hz	40 kHz
1 kHz	next

Low pass filters 270 Hz, 350 Hz, 600 Hz, 1 kHz, 3 kHz, 10 kHz, 20 kHz and 40 kHz can be selected (reference: 3 dB limit frequency). Attenuation of the low pass filters is 20 dB/decade.

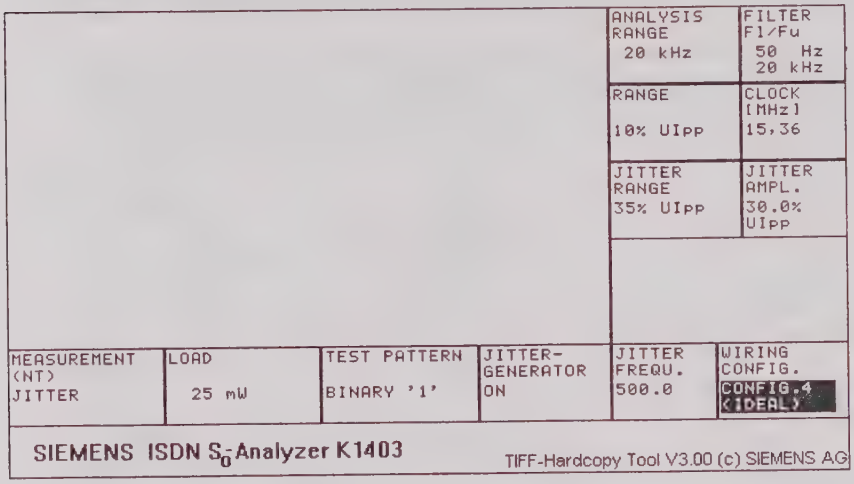
You can either select a new frequency limit or confirm the preset low pass via NEXT.

JITTER GENERATOR

Switching the jitter generator on or off.

JITTER GENERATOR ON

Having switched on the jitter generator you will obtain the following additional setting options:



JITTER FREQUENCY

Die Jitterfrequenz kann im frequency range 0.1 Hz - 20 kHz eingestellt werden.

JITTER RANGE

You can choose between the jitter deviation ranges 35% UI and 70% UI.

JITTER DEVIATION

With the EDIT panel, a jitter deviation of 0.4% UI_{ss} to 35% UI_{ss} can be set for the jitter range 35% UI in steps of 0, 2%UI_{ss} and a jitter deviation of 0.8% UI_{ss} to 70% UI_{ss} can be set for the jitter range 70% UI in steps of 0, 4%UI_{ss}.

For the jitter range 35% UI a jitter deviation of 5% UI is set with the panel 5% UI and for the jitter range 70% UI a jitter deviation of 10% UI is set with the panel 10% UI.

CLOCK.

Depending on the measurement set-up, with this panel an input clock of 12.288 MHz or 15.36 MHz can be selected for the module Option Jitter.

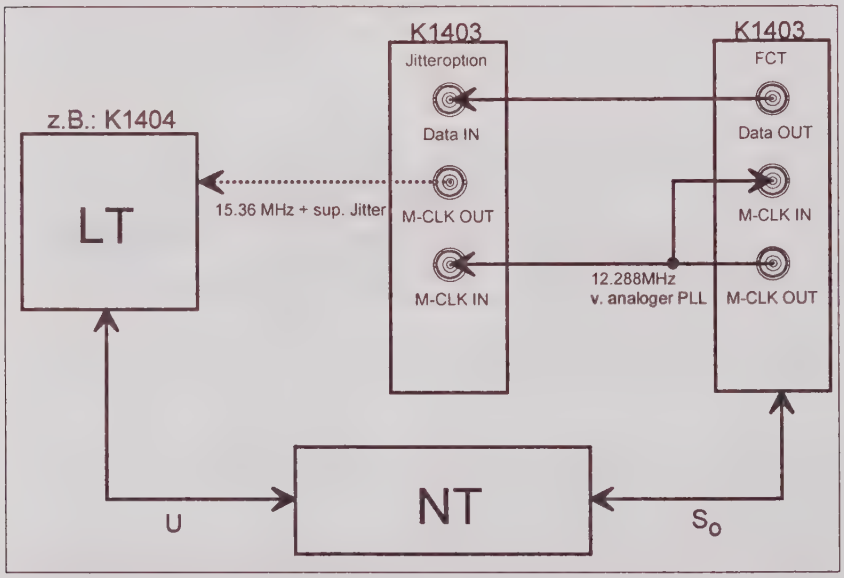
Measurement set-up

The device under test is connected to the K1403 via Bu 6 or Bu7.

Measurement set-up 1:

The reference clock 12.288 MHz for the jitter measurement is achieved in an analog PLL on the module Functional Test L15 and is looped to the clock input of the module Option Jitter L30. This measurement set-up is suitable for jitter measurements with any LT simulator.

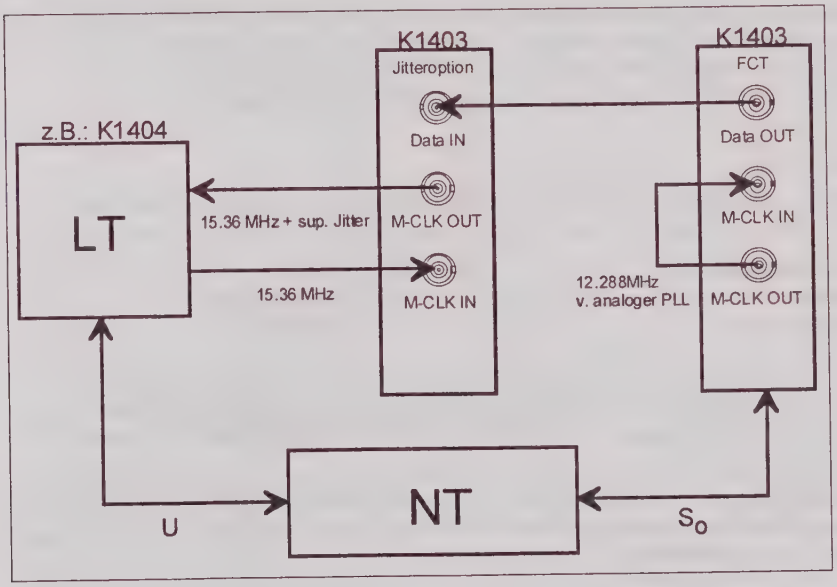
With `JITTER GENERATOR/ON`, a signal with the frequency 15.36 MHz, which is superimposed by the set jitter, is applied to the clock output of the Option Jitter. With that, the transmission output of an LT simulator, e.g. K1404, can be jittered definedly. The jitter amplitude 1 UI corresponds to a time interval of 5.208333 µs.



Measurement set-up 2:

If a K1404 is used as LT simulator, this measurement set-up should be prefered to measurement set-up 1. The reference clock for the jitter measurement is the unjittered master clock of the module Functional Test L33X in K1404.

With `JITTER GENERATOR/ON`, a signal with the frequency 15.36 MHz, which is superimposed by the set jitter, is connected to the clock output of the Option Jitter. With that, the transmission output of the K1404 can be jittered definedly. A jitter amplitude of 1 UI corresponds to a time interval of 5.208333 μs.



Measurement

Start the measurement via the START/STOP key!

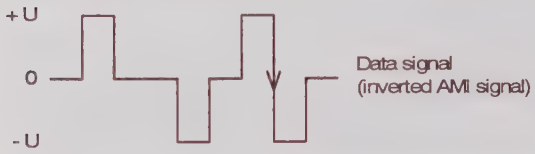
First, the module JITTER is initialized. Then, the following status message "INIT/START" is displayed.

Afterwards, the device under test is activated by way of the module Functional Test. The activation of the TE necessary for jitter measurement is carried out automatically. Following successful activation the jitter measurement is started. The actual start of the measurement is indicated by "MEASURE".

A complete measuring cycle within the selected frequency range inclusive of all calculations, evaluations and the graphic output on the display takes some 1.3 seconds.

Stop the measurement via the START/STOP key. The status message "STOP" will appear in the display. The device under test is brought to state F3.

The input circuit of the phase jitter meter is configured such that the negative going transition of the data signal from +U to -U is used for jitter evaluation.



If the measurement supplement TM-Box (Toolkit) is connected between the device under test and K1403, the jitter of the increasing or simultaneously the jitter of both edges can be measured additionally. The absolute jitter is measured. The unjittered system clock is taken as reference for the measured value assessment.

Result structure

The measured results are displayed in either alphanumeric or graphic form. Numeric display is in the form "n1 n2, n3 %UI". The following measured values are displayed:

- Peak value (peak-peak) x1 x2, x3 %UI_{ss}
- Maximum value of the last 20 measurements y1 y2, y3 %UI_{ss}-Max
- Effective value z1 z2, z3 %UIeff

The display in graphic form is intended for the qualitative evaluation. Within the range of 2 Hz to 20 kHz the phase jitter which has been converted to alternative voltage in the jitter modulator is evaluated without filtering by means of a digital signal analysis.

The analysis range is divided into four ranges of differing frequency grid. The frequency of the lines can be read out by means of a cursor; the Ulss value can be estimated from the diagram.

- Frequency range II comprise the range 10 Hz to 200 Hz with a line grid of 10 Hz and is mainly suited for analysis of system disturbances and their harmonic waves.

- Frequency range I comprises the range 2 Hz to 20 kHz including the three partial ranges a, b and c.

Frequency range II: The amplitude-modulated phase jitter is analyzed in the frequency range from 10 Hz to 200 Hz and is graphically displayed in a line spectrum of 20 lines in intervals of 10 Hz. If a jitter frequency exactly matches one of the lines, this frequency will be exactly presented by this line with regard to both amplitude and frequency:

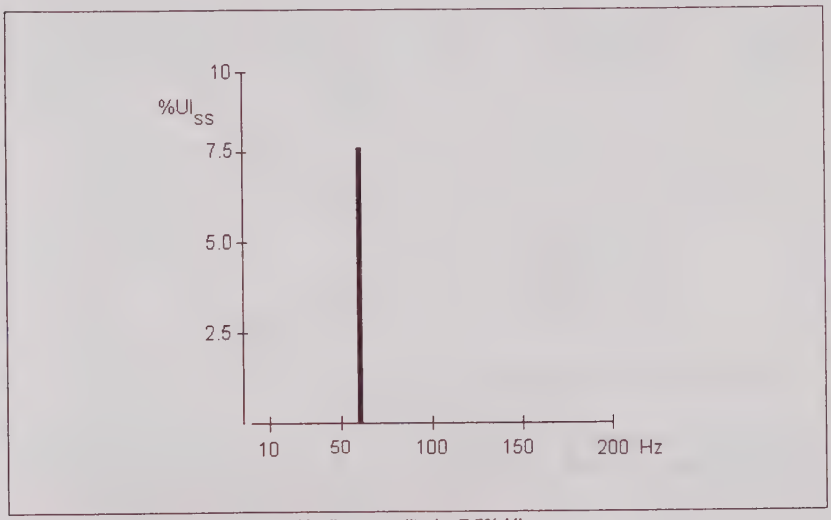


Fig. 5.1: Jitter frequency: 50 Hz; jitter amplitude: 7.5% UI_{ss}

If the jitter frequency does not exactly match any of the lines, two adjoining spectral lines of differing amplitude as well as several exponentially decaying lines will result. The amplitude of the latter reaches a maximum when the frequency to be analyzed is located exactly between two lines. In this case the amplitudes of the two adjoining spectral lines have the same mean value. The exact value of the jitter frequency amplitude (45 Hz) is obtained from:

$$U_{\Sigma} = \sqrt{U_1^2 + U_2^2}$$

The exponentially decaying lines can be neglected when amplitudes are evaluated.

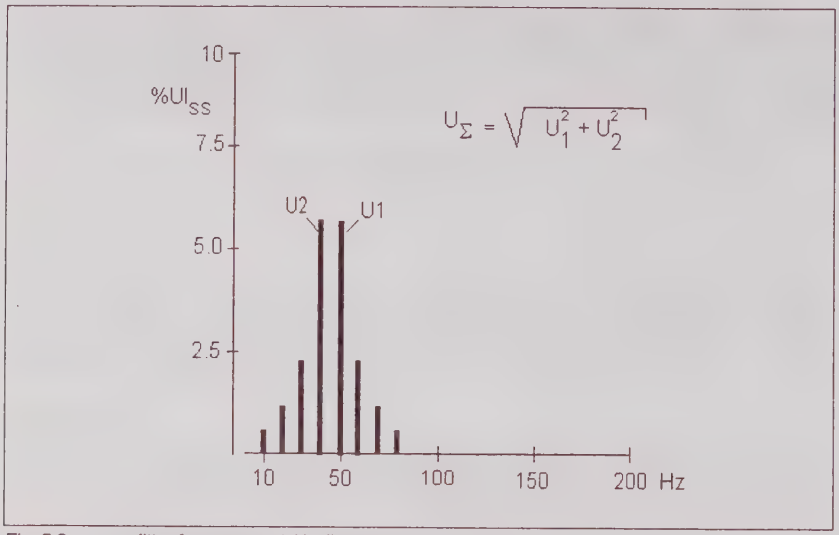


Fig. 5.2: Jitter frequency: 45 Hz; jitter amplitude: 7.5% UI$_{ss}$

If the jitter frequency (49 Hz) is in close vicinity of a line spectrum frequency (50 Hz), the grid line which is closer to the frequency has a higher amplitudinal value than the second one. The exact value of the jitter frequency amplitude (49 Hz) is obtained from:

$$U_\Sigma = \sqrt{U_1^2 + U_2^2}$$

Here, the decay rate of the exponentially decaying lines is higher than in the previous figure.

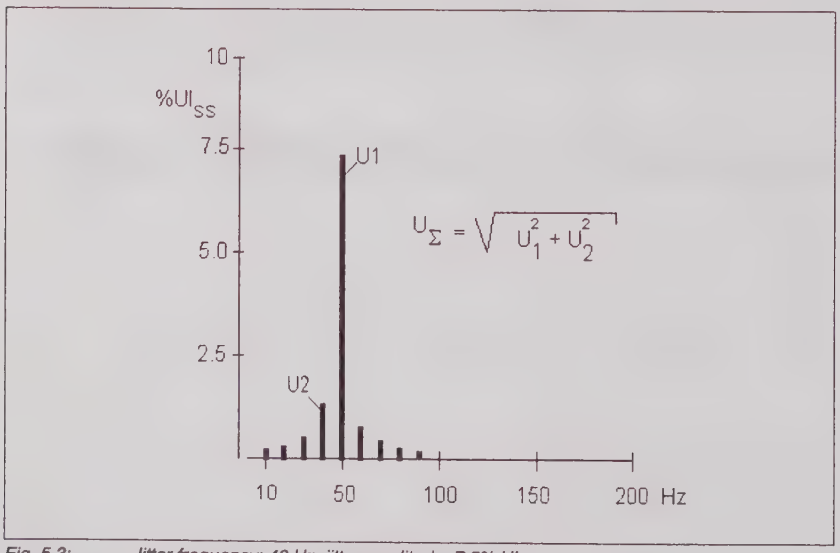


Fig. 5.3: Jitter frequency: 49 Hz; jitter amplitude: 7.5% UI$_{ss}$

Frequency range I (partial range a: 2 Hz to 50 Hz): The amplitude-modulated phase jitter is analyzed in the frequency range from 2 Hz to 50 Hz and is graphically displayed in a line spectrum of 25 lines in intervals of 2 Hz:

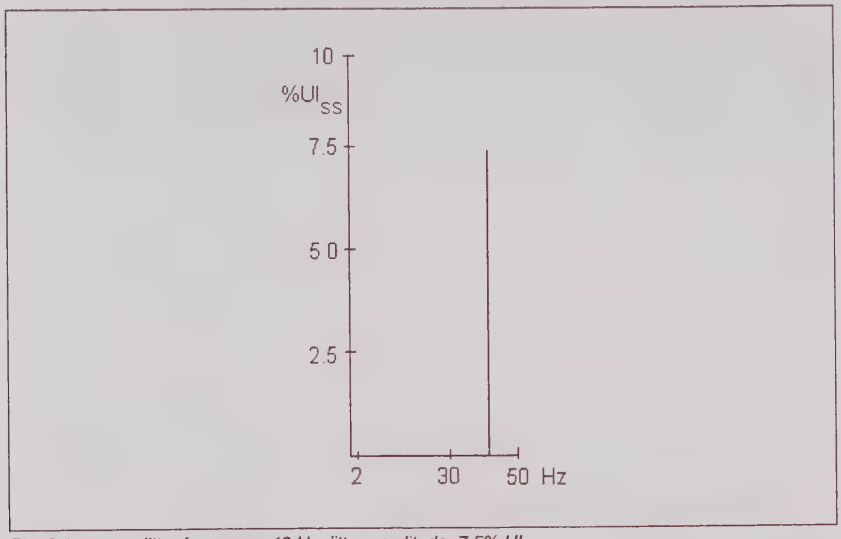


Fig. 5.4: Jitter frequency: 40 Hz; jitter amplitude: 7.5% UI_{ss}

Frequency range I (partial range b: 50 Hz to 1 kHz): The amplitude-modulated phase jitter is analyzed in the frequency range from 50 Hz to 1 kHz and is graphically displayed in a line spectrum of 20 lines in intervals of 50 Hz. A jitter frequency which corresponds to a line spectrum frequency is represented in its exact amplitude. Other frequencies are evaluated and displayed as in "frequency range II":

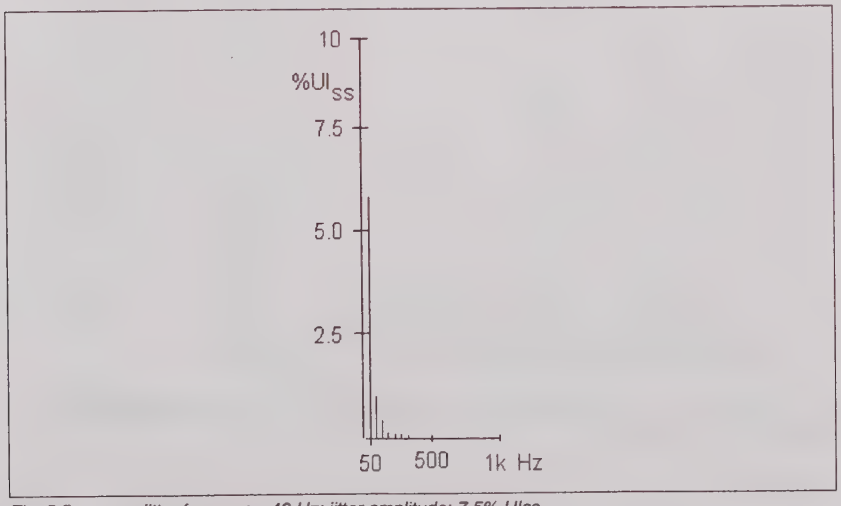


Fig. 5.5: Jitter frequency: 40 Hz; jitter amplitude: 7.5% Uiss

The jitter frequency of 40 Hz does not tally with any of the spectrum lines and is therefore rated with a lower value.

Frequency range I (partial range c: 1 kHz to 20 kHz): The amplitude-modulated phase jitter is analyzed in the frequency range from 1 kHz to 20 kHz and is graphically displayed in a line spectrum of 20 lines in intervals of 1 kHz:

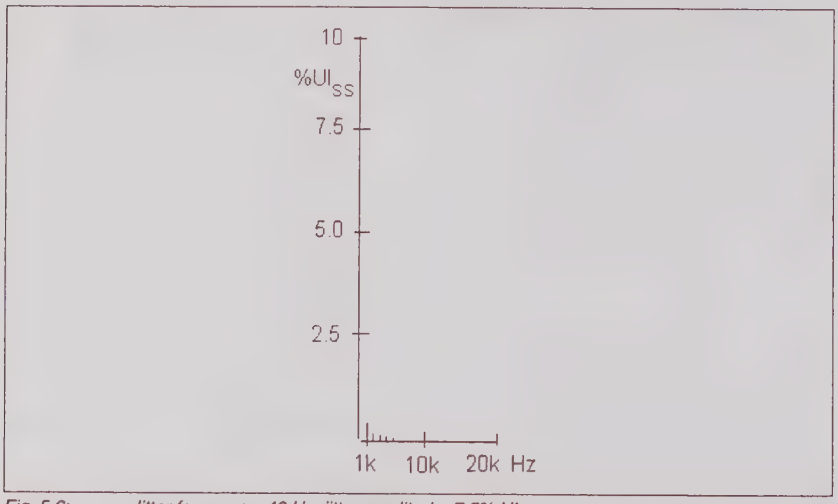


Fig. 5.6: Jitter frequency: 40 Hz; jitter amplitude: 7.5% UI_{ss}

The jitter frequency of 40 Hz does not tally with any of the spectrum lines and is therefore rated with an even lower value than in the previous figure.

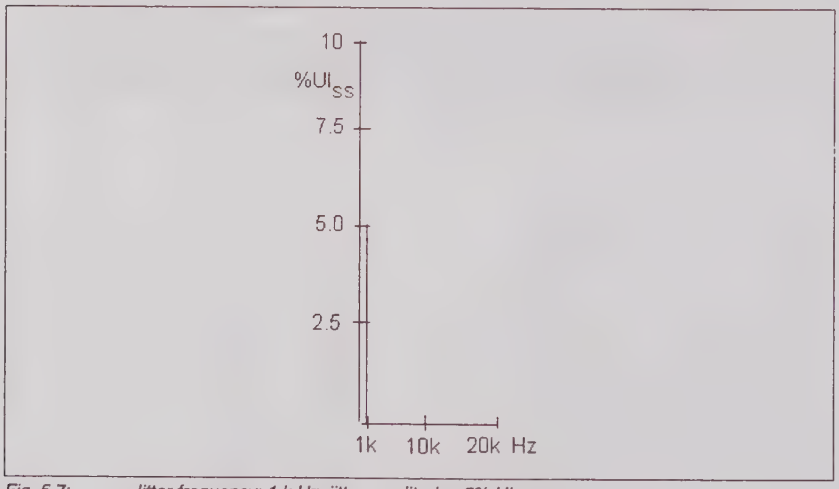


Fig. 5.7: Jitter frequency: 1 k Hz; jitter amplitude: 5% UI_{ss}

The jitter frequency of 1 kHz matches a line of the spectrum and is therefore rated with respect to its full amplitude.

Frequency range I (total range: 2 Hz to 20 kHz): For a better overview, the partial ranges a to c are combined and displayed in a single diagram.

In the case of phase jitter frequencies of 40 Hz and 1 kHz, respectively, all the lines of the partial ranges a to c are contained in the general view. The 1 kHz line is superimposed by a very small spectral line stemming from the 40 Hz spectrum. Due to the quadratic rating this error is so minor that it can be neglected. A thick bar underneath the partial range c (1 kHz to 20 kHz) marks the superimposition by the spectral line at 13 kHz:

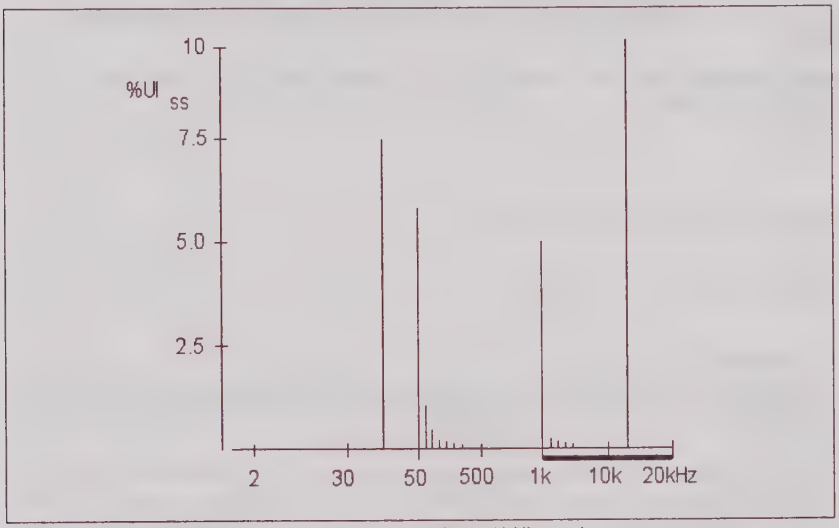


Fig. 5.8: Jitter frequency: 40 Hz; jitter amplitude: 7.5% UIss and 1 kHz, jitter amplitude: 5.0% UIss 13 kHz, jitter amplitude: 15% UIss

Measurements at the jitter demodulator output

The output of the jitter demodulator for measurements with external measuring devices is provided by the BNC socket JITTER. The phase jitter of the device under test can either be analyzed here in its time range by means of an oscilloscope or in its frequency range by means of a spectrum analyzer.

Measurements with oscilloscope: Connect an oscilloscope with an internal resistor of ≥50 ohms to the output JITTER of the jitter module and start the measurement with the desired parameter settings. The display of the oscilloscope will allow you to evaluate line profile, frequency and peak value of the measured phase jitter.

Conversion between measuring voltage at the oscilloscope and phase jitter is according to the equation:

$Dj = k * U$

Dj
Phase jitter of the device under test in UI_{SS}

U
Voltage U_{SS} am at oscilloscope in V

K
Conversion factor in UI_{SS}/V

Measuring range:	k in UIss/V:
0 to 20 %UI_{SS}	3.5714 ±3%
0 to 10 %UI_{SS}	1.7857 ±3%
0 to 5 % UI_{SS}	1.7857 ±3%

A measurement featuring an ISDN telephone as the device under test is displayed in the following form:

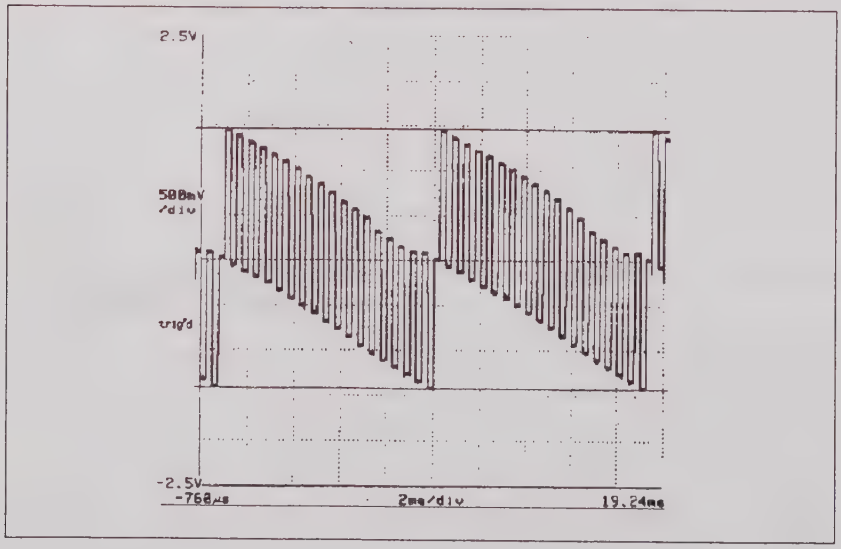


Fig. 5.9: Device under test ISDN telephone; oscilloscopic display of phase jitter with 2ms/div time range

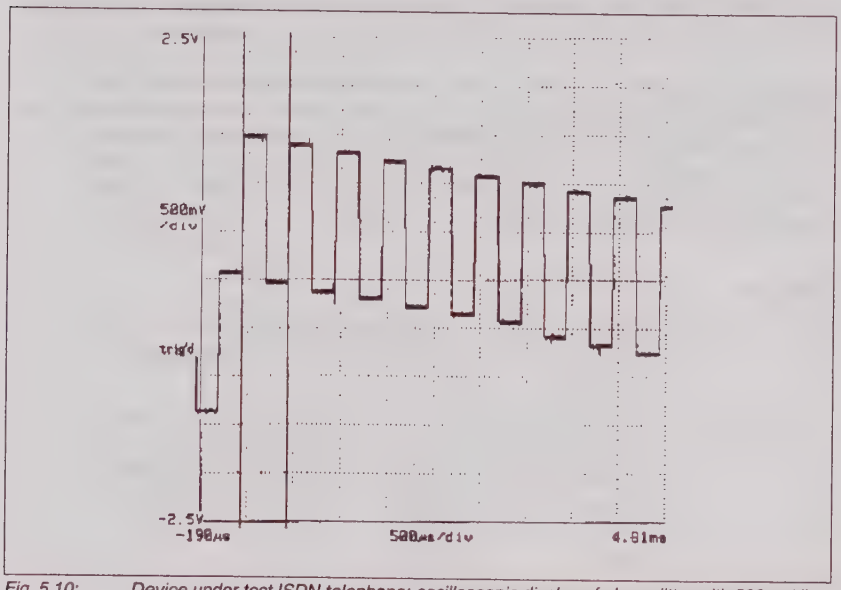


Fig. 5.10: Device under test ISDN telephone; oscilloscopic display of phase jitter with 500ms/div time range

The displayed function of the phase jitter measured at the device under test (transmitting side of the ISDN telephone) consists of a saw-tooth function with a frequency of approx. 107 Hz (see figure above) and a symmetrical rectangle with a frequency of 2 kHz (see figure below). The phase jitter of the saw-tooth function amounts to (1.46V*1.786 % UI_{SS}/V) approx. 2.6% UI_{SS}. The phase jitter of the rectangular function amounts to (1.4V*1.786 % UI_{SS}/V) approx. 2.5%UI_{SS}. A phase jitter of approx. 5.1 % UI_{SS} results.

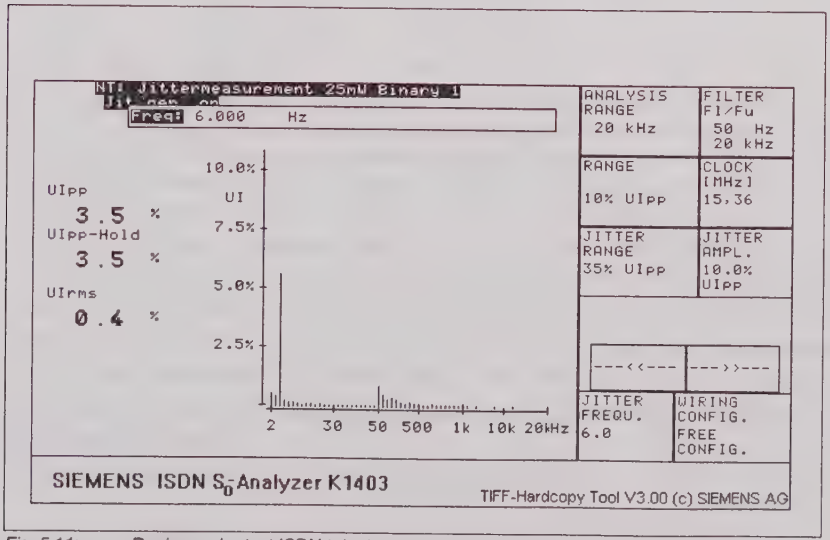


Fig. 5.11: Device under test ISDN telephone; display of phase jitter at K1403

The peak-to-peak evaluation, the maximum peak-to-peak evaluation comprising 20 measurements as well as the effective evaluation of the measured phase jitter can be read. In addition, the spectrum lines of the phase jitter can be read from a diagram using the cursor.

The peak-to-peak value of the phase jitter cannot be derived from the spectral lines, because the phase information between the individual spectral lines is missing. Within the spectrum, the 6 Hz line generated by the jitter generator can be seen clearly. The clock recovery in the device under test reduces the 10 % UI_{ss} jitter deviation of the generator by 4.4 %UI_{ss} to 5.6 %UI_{ss}. This corresponds to a jitter suppression of 5 dB for a frequency of 6 Hz.

Error meassages

`NO SIGNAL`	After the start no signal is displayed during the synchronization process and when the data signal is missing.
`JIT: NO MEASURING`	The jitter measurement is due to begin but cannot be started owing to a setting or parameter error. In this case the measurement must be stopped and restarted. If the error is continously displayed, either the jitter module or the main CPU is defective. (IEC error no. 302)
`JIT: SET UP ERROR`	Like `JIT: NO MEASURING`, however, without activated jitter measurement; i.e. only the jitter generator is used. (IEC error no. 304)

Calculation of the jitter transmission function

The following paragraphs will tell you how to calculate the jitter transmission function from the measurements ABSOLUTE JITTER MEASUREMENT and RELATIVE JITTER MEASUREMENT.

ABSOLUTE JITTER MEASUREMENT (JITTER GENERATOR ON):

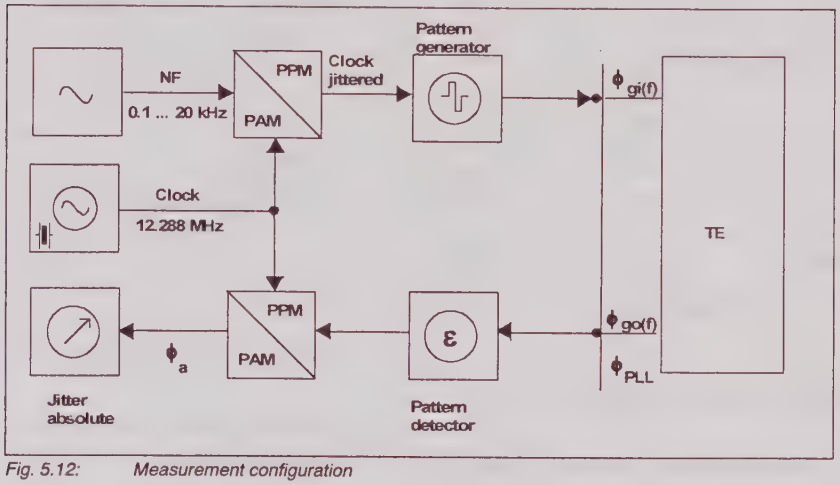


Fig. 5.12: Measurement configuration

ϕ_a
absolutely measured phase jitter

$\phi_{gi}(f)$
phase jitter of the jitter generator at the input of the TE with frequency (f)

$\phi_{go}(f)$
residual phase jitter of the jitter generator at the output of the TE with frequency (f)

ϕ_{PLL}
phase jitter caused by the clock recovery circuit in the TE

If ABSOLUTE JITTER MEASUREMENT is selected, the unjittered clock of 12.288 MHz is used both in the jitter modulator for generating a defined jittered clock and in the jitter demodulator as a reference clock for jitter demodulation. The clock of the pattern generator (192Hz) is derived from the jittered clock of 12.288 MHz so that the data stream to the TE is jittered in defined form with the jitter $\phi_{gi}(f)$. In the TE, the clock for the transmission data is recovered from the jittered data stream in a clock recovery circuit (PLL) which partly suppresses the jitter of the receiving data. The transmission data contains the unsuppressed residual jitter $\phi_g(f)$ of the receiving data as well as an additional jitter ϕ_{PLL} resulting from the clock recovery. In the jitter demodulator, the data stream with the jitter ($\phi_g(f) + \phi_{PLL}$) is demodulated by means of the jitter-free clock of 12.288 MHz and is displayed on the device as "absolute jitter".

The following equation applies to the absolute phase jitter:

$$\phi_a = \phi_{go}(f) + \phi_{PLL}$$

RELATIVE JITTER MEASUREMENT (JITTER GENERATOR ON):

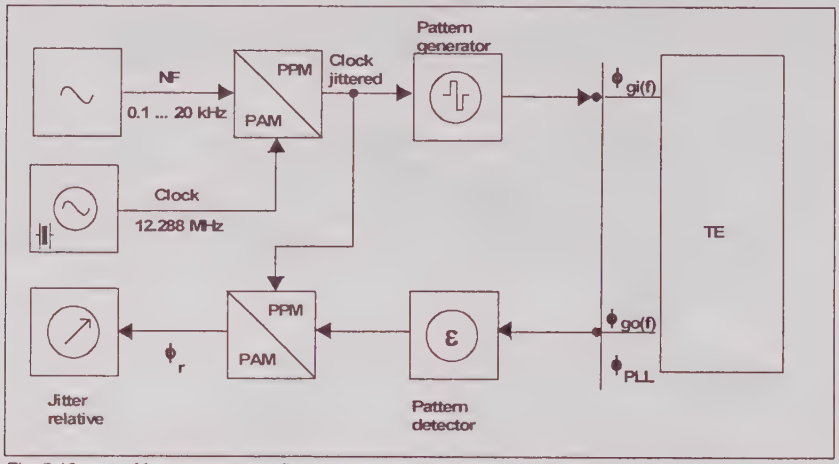


Fig. 5.13: Measurement configuration

ϕ_r
relatively measured phase jitter

$\phi_{gi}(f)$
phase jitter of the jitter generator at the input of the TE with frequency (f)

ϕ_g (f)
residual phase jitter of the jitter generator at the output of the TE with frequency (f)

ϕ
phase jitter caused by the clock recovery circuit in the TE

If RELATIVE JITTER MEASUREMENT is selected, the unjittered clock of 12.288 MHz is used in the jitter modulator for generating a defined jittered clock. This jittered clock is used in the jitter demodulator as reference clock for the jitter demodulation. The clock of the pattern generator (192 kHz) is derived from the jittered clock of 12.288 MHz so that the data stream to the TE is jittered in defined form with the jitter $\phi_{gi}(f)$.

In the TE, the clock for the transmission data is recovered from the jittered data stream in a clock recovery circuit (PLL) which partly suppresses the jitter of the receiving data. The transmission data contains the unsuppressed residual jitter ϕ_g (f) of the receiving data as well as an additional jitter ϕ resulting from the clock recovery. In the jitter demodulator, the data stream with the jitter (ϕ_g (f) + ϕ) is demodulated by means of the jittered clock of 12.288 MHz and is displayed on the device as "relative jitter". In the event of an ideal jitter suppression by the clock recovery circuit, the measured realative jitter corresponds to added values of the phase jitter of the jitter generator ($\phi_{gi}(f)$) and the jitter (ϕ) resulting from the clock recovery. The following equation applies to the measured relative jitter ϕ_r:

$$\phi_r = \phi_{gi}(f) - \phi_{g0}(f) + \phi_{PLL}$$

Calculation

The residual jitter ϕ_g (f) and the jitter transmission function F_j(f) of the clock recovery circuit in the TE can be calculated on the basis of the measurement of the absolute and relative jitters with reference to the following formulas. Here, both the residual jitter and the jitter transmission are a function of the jitter frequency of the jitter generator:

$$\phi_{g0}(f) = \frac{\phi_{gi}(f) + \phi_a - \phi_r}{2}$$

and

$$F_j(f) = 20\lg \frac{2\phi_{gi}(f)}{\phi_{gi}(f) + \phi_a - \phi_r}$$

ϕ_a
absolutely measured phase jitter

ϕ
relatively measured phase jitter

ϕ (f)
set phase jitter of the jitter generator at the input of the TE with frequency (f)

ϕ (f)
residual phase jitter of the jitter generator at the output of the TE with frequency (f)

F_j(f)
jitter transmission function

6 Appendix

On the following pages you will find the technical data for the jitter module.

6.1 Technical Data

6.1.1 Jitter

Jitter generator

Jitter frequency	
Range	0.1 Hz to 199.9 Hz, adjustable in steps of 0.1 Hz 200 Hz to 20 kHz, adjustable in steps of 1 Hz
Basic error	$\Delta f/f \leq 1 * 10^{-4}$
Jitter amplitude	Sinusoidal
Range I	0.4% UIss to 35 % UIss, adjustable in steps of 0.2 % UIss Error at 1 kHz: 1 % of measured value
Range II	0.8% UIss to 70 % UIss, adjustable in steps of 0.4 % UIss Error at 1 kHz: 2 % of measured value
Jitter frequency response flatness	Referred to the jitter amplitude at 1 kHz Up to 5 kHz : 1% UIss Up to 10 kHz : 3% UIss Up to 20 kHz : 10% UIss
Clock output	BNC socket
Output impedance	< 4 Ω
Signal level	4 V<U<5 V into Rout ≥ 75 Ω
Clock frequency	12.288 MHz / 15.36 MHz

Jitter meter

Evaluation I

Presentation of results	UIss, UIss-max and UIeff numeric
Measuring range I	0 to 20 % UIss or 0 to 7.0 % UIeff Error in displayed jitter at jitter frequency of 1 kHz
Jitter frequency:	1 % ± 0.3 % UIss
Measuring range II	0 to 10% UIss or 0 to 3.5 % UIeff Error in displayed jitter at jitter frequency of 1 kHz
Jitter frequency:	1 % ± 0.2 % UIss
Measuring range III	0 to 5 % UIss or 0 to 1.7 % UIeff Error in displayed jitter at jitter frequency of 1 kHz
Jitter frequency:	$2\% \pm 0{,}2\% UI_{SS}$
Display resolution	0.1 % UIss or 0.1 % UIeff

Band limitation	Selectable for fmin and fmax High-pass: 3dB cut-off frequency: f_{min}: < 1,5,10,15,30,50,80,110 Hz Attenuation characteristic in the stop band: 20 dB / decade Low-pass: 3dB cut-off frequency: f_{max}: 40,270,350,600Hz; 1,3,10,20,40kHz Attenuation characteristic in the stop band: 20 dB / decade

Evaluation II

Presentation of results	Spectral components of jitter signal (graphical)
Frequency range I	2 Hz < f < 20 kHz Subrange a Up to 50 Hz with 2 Hz divisions Subrange b Up to 1 kHz with 50 Hz divisions Subrange c Up to 20 kHz with 1 kHz divisions
Frequency range II	10 Hz < f < 200 Hz up to 200 Hz with 10 Hz divisions
Repetition rate	Approx. 1.5 s

Signal input

For jitter meter from K1403 basic unit or external signal source

Input voltage	Uss = 2 V (192 kbit/s, AMI) at 500 Ω
Input socket	BNC

Clock input

For jitter meter and jitter generator from K1403 basic unit or external signal source e.g. K1404

Input voltage	Uss = 4 V

Reference clock

12.288 MHz / 15.36 MHz

Input socket	BNC

Jitter demodulator output

For jitter analysis with external equipment

Output socket	BNC
Output impedance	< 4 Ω
Signal voltage	K1403 measuring range: 0 to 20% Ulss Ulss = 0 to 5.6 V 0 to 10% Ulss Ulss = 0 to 5.6 V 0 to 5% Ulss Ulss = 0 to 2.8 V

SIEMENS

ISDN S_0 Analyzer K1403

Functional Tests

User Manual C73000-B6076-C57-3

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CE

The product described in this manual complies with the statutory regulations on electromagnetic compatibility of devices (EMC) or the regulations of the guideline of the council from 03.05.1989 for adaptation of the statutory regulations of the member countries on electromagnetic compatibility of devices (89/336/EEC).

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1 Safety information

The ISDN S_0 Analyzer K1403 has been constructed and tested in accordance with Publication EN61010 Safety Provisions for Electronic Measuring Equipment, and has left the factory in a perfectly safe condition. In order to maintain optimum safety and ensure hazard-free operation, please adhere to the following basic rules.

- Transport the device only in its original packing or by using the transport case specially recommended for the K1403. This will protect the device against shocks.
- The K1403 is exclusively intended for indoor use. Condensation may occur when the unit is brought to its site of operation from a cold environment. Operation is only permissible with an absolutely dry unit after its temperature has adjusted to the environment.
- Before implementing and operating the K1403, make sure that the environmental conditions are complied with. The environmental conditions are listed under the heading "Technical data" in the appendix.
- Before switching on the device, make sure that the preset operating voltage of the device corresponds to the permissible line voltage.
- Make sure that replacement fuses are of the specified type and rating: Use 3.15A/250 V (type T) fuses.
- The power plug must only be inserted into a grounded socket. Do not cancel the protective effect by using an extension cable without a protective ground conductor.
- Make sure that the ventilation slots on the rear and top of the device are not covered.
- The unit can become dangerous if the protective ground conductor is interrupted either inside or outside the unit. Do not interrupt the protective ground conductor intentionally. The same applies when loosening the connection for the protective ground conductor. When opening covers or removing parts, remember that live parts may be exposed if the unit is connected. Connection points may also be live. Disconnect the unit from all voltage sources prior to adjustment, maintenance , repair or when replacing parts. If such work on live and open units cannot be avoided, it should only be performed by qualified staff familiar with the hazard involved.

- All modules contain electro-sensitive components. Please note the necessary precautions and ESD safety measures :

Warning!

When electrical devices are in operation certain parts of these device are live. Non-observance of the above precautions may therefore lead to severe physical injuries or to serious material damage.

Only qualified staff may handle this device or work in its vicinity. They must be thoroughly familiar with all the warnings, safety and maintenance information contained in these instructions. Faultless and safe operation of the device presupposes proper transport, proper storage, set-up and mounting as well as careful handling and servicing.

2 Device description

2.1 Functional tests

The module "Functional tests" (FCT) designed for the ISDN S_0 analyzer K1403 enables all measurements recommended by the CCITT and defined by ETSI and CTS to be carried out for layer 1 of the ISDN base connection. In addition to the bit-by-bit construction and analysis of the S_0 frame, these measurements include the defined activation and deactivation procedures of layer 1. The functional test module, can be operated in two different modes: it operates in TE mode like conformal terminal equipment (TE) and in NT mode like a network terminator (NT).

The tests based on the CTS-2 test specifications can be combined into 10 groups which are described in detail in Section 5.

I. ***Basic interconnection tests :*** The ability of the test object to carry out elementary layer 1 procedures is checked, e.g. send Info3 if Info2 has been received (in TE mode).

II. ***Binary organization of frame :*** The received bits of the S_0 signal are displayed graphically in envelope mode. Bit-by-bit analysis of the S_0 frame is then possible.

III. ***Interframe time fill :*** This test analyzes the D-channel data in real time.

IV. ***D-Echo channel procedure :*** The access of terminal equipment to the D-channel commences with successful execution of the procedure described by CTS_9.1. The procedures are verified by specific control of the echo bit.

V. ***Activation/deactivation procedure :*** Each change in status of layer 1 is programmed on the module. The layer 1 activation and deactivation procedures defined by CTS are verified.

VI. ***Timer tests :*** The timing conditions of layer 1 are checked and recorded using the procedures described in TTCN.

VII. ***Frame alignment procedures :*** The module sends the *good/bad frames* defined according to CTS for Frame alignment/loss and records the status of the test object depending on the received information.

VIII. ***Multiframing procedures :*** The Q bit is compared with the transmitted FA bit and recorded.

IX. ***Idle channel code on the B-channels :*** Terminal equipment already activated in layer 1 must not send data in the B-channels until the channels are enabled by the higher layers. This *B-channel monitoring* test is only carried out on the TE, the test duration is 100 ms.

X. ***Receiver sensitivity, noise and distortion immunity :*** A PRBS signal is sent during the test and the bit error count BEC and rate BER measured for the duration of 1 minute with the loop switched on or in test mode of the test object. The transmitted amplitude can be set between -8 and +3 dB in increments of 0.1 dB.

Design and Mode of Operation

The design and mode of operation of the functional tests module which will be referred to as L15 hereafter are described below.

The complete SIEMENS part no. of the module is C73249-A11-L15-1.

Processor

The functional tests module has two MCS-51-compatible *single-chip microcontrollers* UPI-452. Processor 1 is largely responsible for the layer 1 measurements such as e.g. data coupling-in/out, synchronization, info recognition etc. Processor 2 is used to handle the protocol software for the higher layers. By switching over the FIFO interface, Processor 1 can use Processor 2 as a *quasi-slave controller* and thus synchronize the layer 1 sequences with the higher layers.

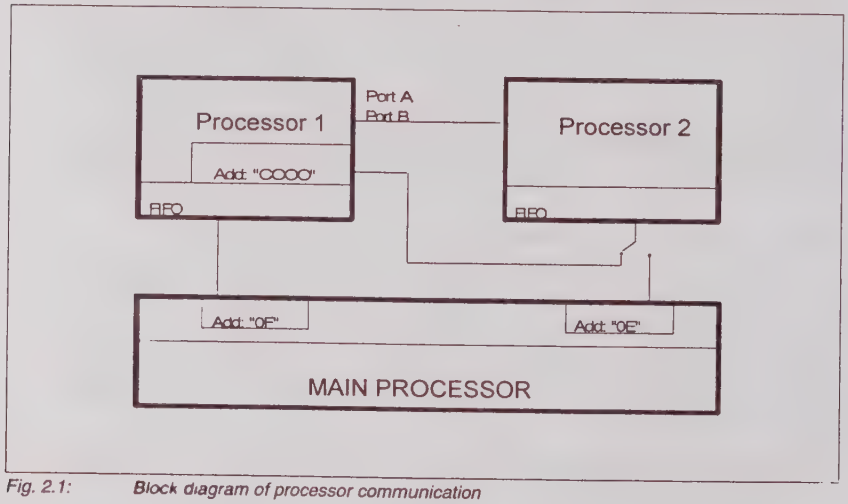


Fig. 2.1: Block diagram of processor communication

Each processor has a V.24 interface for the hardware settings. X120 and X170 are the sockets for the V.24 interface and have the following pin assignments:

n.c.	1	2	n.c.
TXD	3	4	GND
RXD	5	6	GND
CTS	7	8	GND
RTS	9	10	GND

Fig. 2.2: Pin assignments of 10-way serial interface

Processor 1 is provided with a crystal clock. The clock frequency of f_{osc} = 11.0592 MHz is present at the oscillator output of the processor and is connected to the clock input of the second processor. The latter is thus provided with a synchronous clock from the first processor. The processor is reset by connecting the power supply "*power-on reset*" and also by applying a "high level" to the UPI_RST input (X11/5) of the processor interface.

Processor 2 also has an external V.24 interface accessible on the rear panel.

The pin assignments of the external V.24 socket are listed below:

Pin	Symbol	Name
2	RXD	received data
3	TXD	transmitted data
5	GND	signal ground
7	RTS	request to send
8	CTS	clear to send

Pin assignments of 9-way serial interface

The hardware addresses of the L15 module are in the top 32-K address range from "8000H" to "FFFFH". 2K are reserved for each of the 16 hardware addresses.

The address divisions are shown in the following table:

Chip select	Address area	Function
CS0	8000-87FF	ISDN layer 1 chip
CS1	8800-8FFF	Dual-port Ram
CS2	9000-97FF	Pattern generator/detector
CS3	9800-9FFF	Clock generator
CS4	A000-A7FF	Vacant
CS5	A800-AFFF	EEPROM
CS6	B000-B7FF	REC_ROM for L1 chip
CS7	B800-BFFF	D/A converter
CS8	C000-C7FF	FIFO
CS9	C800-CFFF	D-/echo channel control
CS10	D000-D7FF	PIOP for HW setting
CS11	D800-DFFF	PIOP for HW setting
CS12	E000-E7FF	Interrupt control
CS13	E800-EFFF	Vacant
CS14	F000-97FF	Vacant
CS15	F800-9FFF	Vacant

CS Memory division

Clock Generation, PLL

The bit clock and the frame clock for data coupling-in/out are generated on the L15 module. The clock is synchronous with the received signal on the S_0 bus.

The possible frame clock and bit clock settings FSC/CLK are:

* FSC : 4kHz, 8kHz, 16kHz, 32kHz
* CLK : 4kHz, 8kHz, 16kHz. 32kHz, 64kHz, 96kHz, 128kHz, 192kHz

In addition to the digital clock recovery, the L15 module also has an analog PLL. The jittered 192-kHz clock recovered from the received signal is applied to the analog PLL. In the case of jitter frequencies above 10 MHz, the jitter amplitude is suppressed by more than 30 dB. The amplitude of the remaining jitter is approx. 20 ns (< 0.005 UI). A signal generated by the digital clock recovery and with the jitter suppressed by the analog PLL is thus available in TE mode at the BNC socket "M-CLK Out". In NT mode, the master clock of the module is present at the same socket. The frequency is 12.288 MHz in both modes with CMOS level.

The clock at the socket "M-CLK out" can be applied to a jitter modulator. The optional module Jitter 7KK1403-2AB00 is ideally suited for this application. The signal modulated by a jitter amplitude and frequency at 12.288 MHz is connected to the socket "M-CLK in". The menu setting external frequency means that the clocks on the transmitter side are derived from this clock and thus transmitted with the set jitter amplitude and frequency.

The socket "data out" is located on the rear panel of the module in addition to the sockets for clock input and output. The electrically decoupled received signal is amplified 1, 1.7, 2.8 or 4.7 times depending on the received level and is available at this socket. The two signals "data out" and "M-CLK out" can be applied to an external jitter test set in order to verify the jitter amplitude and frequency of the received signal.

Data coupling-in/out

Shift registers are required for data coupling-out which convert the data from burst mode to continuous mode. This is achieved by reading the data of the set channel on the S_0 bus using a burst clock and storing them temporarily in the burst mode register. Following transfer of the data to the continuous mode register, they are transmitted serially with the continuous clock. On the other hand, the data during data coupling-in is converted from continuous mode to burst mode and applied to the set channels.

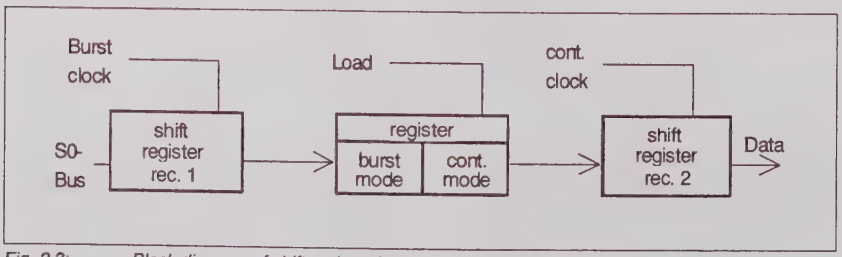


Fig. 2.3: Block diagram of shift register for data coupling-out

A multiplexer is connected in series with the shift register used for data coupling-in.

The following data sources are available for this purpose:

* Internal data source: bit pattern generator/detector

Pseudo-random binary sequences (PRBS) 2^9-1, 2^{11}-1, 2^{15}-1, 2^{20}-1

* Data from socket 2

The data at the contradirectional interface on the K1403 (BNC sockets BU2 and BU3 on front panel) are coupled-in

* Dout = Din

Data loop; the received data are coupled-out and coupled-in into the set channels

* EEPROM data

The data from the internal non-volatile memory are coupled-in.

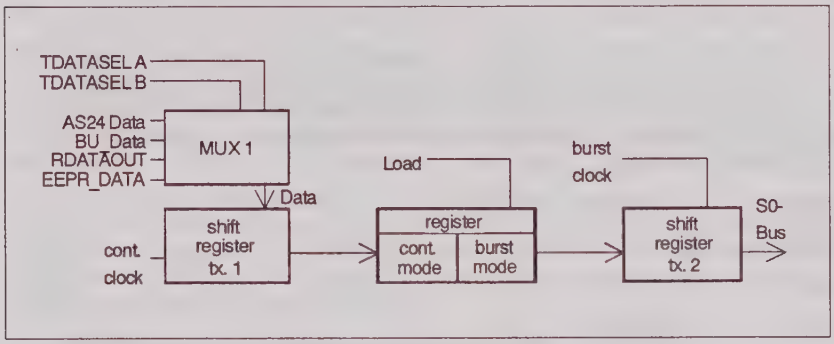


Fig. 2.4: Block diagram of shift register for data coupling-in

The transmitter of the bit pattern generator and the receiver of the bit pattern detector are clocked using the same continuous clock. The transmitter can also be clocked with the burst clock for the event that no bit error rate measurements are required. It can then be operated with other clock frequencies such as e.g. the setting of the 144-kHz transmitter clock with PRBS coupling-in in the B1+B2+D-channels. The bit error rate measurement is not possible in conjunction with the burst clock on the bit pattern generator/detector.

Four BNC sockets are located on the front panel of the K1403. Sockets BU_2 and BU_3 are used for data coupling-in/out, sockets BU_4 and BU_5 for the bit and frame clocks. The outputs have CMOS level.

The NRZ signal prepared for transmission and reception by the shift register sequences must satisfy other important criteria before it is applied to the transmitter frame. These criteria include the inherent jitter, the phase position, the AMI coding and the L-bit control.

Coupling-in of five different data channels is possible; these can be configured together as desired. In practice, however, only the following combinations are possible for the data coupling-in on the S_0 bus.

A total of seven different configurations can be selected according to the following table:

Channel	Bit rate (kHz)
S1,2	8
D	16
E	16
B1	64
B2	64
B1+B2	128
B1+B2+D	144

Coupling-in possiblities of the channels

Coupling-out possibilities are available corresponding to the coupling-in possibilities mentioned above and are achieved with the exception of the (B1+B2+D) channel by addressing the layer 1 component.

The D_echo channel can be switched off in NT_mode if required. With the echo loop switched on, L15 decouples the D-channel data at the receiver end and returns them in the echo bits. The coupled-out D-channel bits can also be modified specifically and subsequently transmitted. There are four different possibilities for coupling-in of the D_echo channel data

* D_echo= D-channel data (receiver side)
* D_echo= inverted D-channel data (receiver side)
* D_echo= fixed level "L"
* D_echo= fixed level "H"

This possibility enables the access control of terminal equipment to be tested in addition to the priority class.

In the NT_test, the received D_echo bits are compared with the transmitted D bits. Errors are detected and indicated.

The Receiver sensitivity is measured at various transmitted levels. The module has an 8-bit D/A converter; the transmitted amplitude is determined at the converter output. The minimum transmitted level is 275 mV, the maximum 1096 mV. The transmitted signal can also be inverted.

Jitter and Phase Delay

In TE mode, the transmitted clock of the L15 module is derived from the received signal. This clock recovery is achieved using a digital PLL with a residual jitter of 1.56 % UI.

The phase delay can be adjusted in TE mode between 1.0 UI and 8.625 UI in increments of 1/64 UI.

Dual-port RAM and EEPROM Control

The coupled-out, AMI-coded S_0 bus signal is decoded as a POS, NULL, NEG signal. This data is written into a dual-port RAM by means of a sequence control implemented as an EPLD, and evaluated by Processor 1 following the measurement.

The dual-port RAM used has a memory depth of 2 Kbyte which can be configured as a ring buffer with a length of either 1, 16 or 32 frames. The data is written into the ring buffer until the measurement is stopped. Depending on the selected configuration of the memory depth, the memory contains the decoded S_0 signals of the last frame, the last 16 frames or the last 32 frames as well as the O rings of these signals at the same bit position during the complete measurement procedure.

It is advantageous for certain applications to couple-in the previously applied data. The data are applied to the non-volatile EEPROM in two steps. In the first step, the data applied to socket BU2 are read by Processor 1 using an intermediate sequence control and stored in its data memory. In the second phase, the data is transferred from the main memory to the EEPROM.

The data stored in the EEPROM is read either in four 8-Kbyte blocks or in one 32-Kbyte block. The reading of each individual block takes one second at a transmission rate of 64 kbit/s. Thus, for example, a digitized voice signal up to 4 seconds long can be applied to the B-channels.

ICC Control, IOM Interface

The L15 module has an ICC component PEB2070 for handling the protocols of layers 2 and 3. It communicates with the layer 1 components via the IOM interface. The serial port b (SPb) of the PEB 2070 is the IOM interface which is used either in "Timing mode 0" as terminal equipment or in "Timing mode 1" as the network.

The D-channel data obtained from the S_bus is coupled-in into the time slots in the IOM frame in the ICC direction. The D-channel contents of the IOM frame in the layer 1 direction are coupled-out with the IOM D-channel burst and applied to the associated S_bus time slots. The frame clock of 8 kHz and the bit clock of 512 kHz are also generated by the sequence control.

The phase of the generated frame clock FSC is 6 UI earlier (1/8 frame period) in "Timing Mode 1" than in "Timing mode 0".

Interfaces

The L15 module is connected to the basic unit via two 62-way direct plugs. The names and functions are described below.

X10	Processor bus	Printed side
X11	Processor bus	Component side
X20	Analog bus	Printed side
X21	Analog bus	Component side

	Printed side X10	Component side X11	
	.	.	
GND	3	3	GND
VCC	4	4	VCC
	.	5	UPI_RST
	.	.	
	.	10	UPI_CS
UPI_A12	11	11	UPI_A11
UPI_A14	12	12	UPI_A13
	..	13	UPI_A15
	..	..	
	17	17	UPI_IN
UPI_RD	19	19	UPI_WR
UPI_A1	20	20	UPI_A0
	..	21	UPI_A2
	..	..	
UPI_A8	23	..	
UPI_A10	24	24	UPI_A9
UPI_D0	25	25	UPI_D1
UPI_D2	26	26	UPI_D3
UPI_D4	27	27	UPI_D5
UPI_D6	28	28	UPI_D7
	..	..	
	..	..	

Pin assignment of processor interface

	Printed side X20	Component side X21	
	..	..	
GNDA	6	6	GNDA
	.	..	
NT/TE_N	10	10	
TRIGGER IN/OUT	11	11	
REC(+)	15	15	REC(-)
TX (+)	16	16	TX (-)
	..	..	
V12P	19	19	V12P
V12N	20	20	V12N
BU 2	21	21	BU 4
BU 3	22	..	
	..	..	
	..	27	BU 5

Pin assignment of measuring bus interface

Block diagram

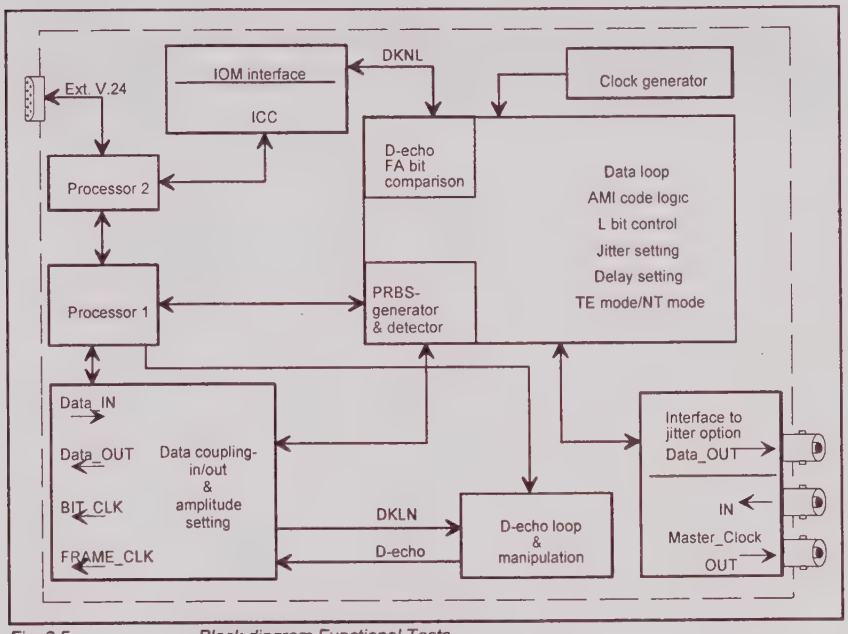


Fig. 2.5 *Block diagram Functional Tests*

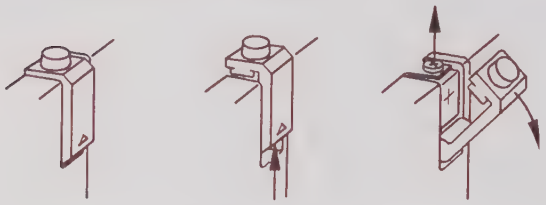
3 Start-up preparations

The following pages will tell you how to make the ISDN S_0 Analyzer ready for use. It will also tell you what you must observe when mounting the K1403 modules.

3.1 Mounting a module

First, remove the cover of the device. The fixing screws for the cover are covered by four corner latches. Proceed as follows:

➤ Push the corner latches some 4 mm upward in direction of the arrow and unhinge the corner latches.



➤ Loosen the four screws which are now accessible and remove the cover.

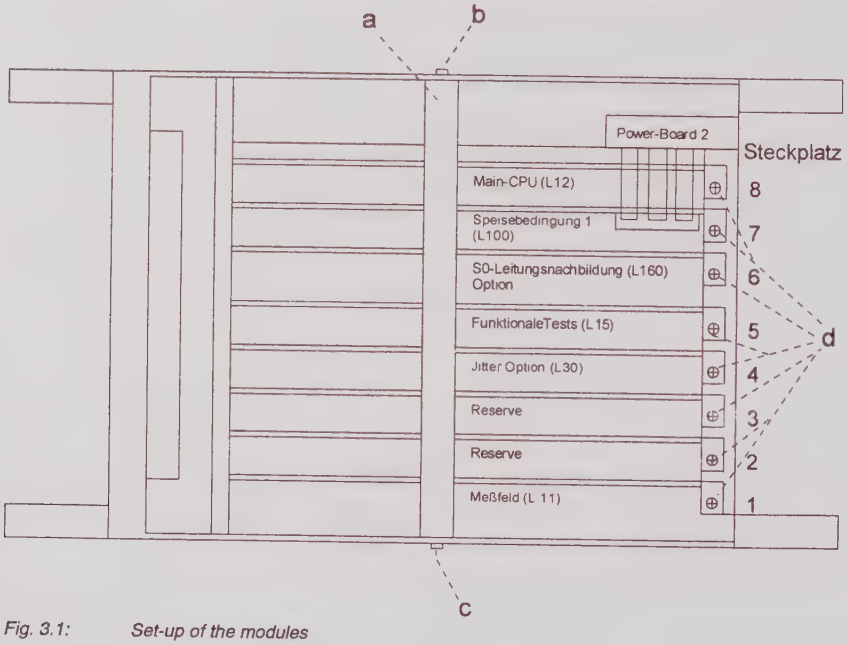


Fig. 3.1: Set-up of the modules

➤ Take the support (a) out by removing screws (b) and (c).

➤ Loosen the module slot screw (d). Insert the module into its destined slot. Ensure that it is correctly assigned and properly fitted in the guide support.

➤ Tighten the module slot screw (d). Re-mount the support (a): Position the printed board in the grooves of the support and tighten screws (b) and (c).

➤ Re-attach the cover of the device.

3.2 External Connections

The typical configurations for application of the functional test module are described below. The jitter option 7KK1403-2AD is ideal for use with a jitter test set or jitter generator since these two functions are present on one module and can be controlled very simply using the K1403 menu. For example, in the measuring mode Receiver sensitivity it is possible to set the required superimposed jitter of the transmitted signal in defined steps of

5Hz / $0.5UI_{pp}$

20Hz / $0.125UI_{pp}$

50Hz / 0.05UIpp

2kHz / $0.05UI_{pp}$

A. Jitter measurement

The following two BNC sockets are connected to a jitter generator, e.g. to the jitter option, to enable measurement of the jitter amplitude and frequency of the received signal.

Data OUT :

The electrically isolated and amplified S_0 bus signal is provided here. The amplitude is amplified up to 4.7 times depending on the S_0 bus level at the receiver end and has an amplitude of approx. 1 V. The S_0 bus bit rate is 192 kHz.

Master_Clock OUT :

This clock is the module-internal system clock. The output has CMOS level. The frequency is 12.288 Mhz.

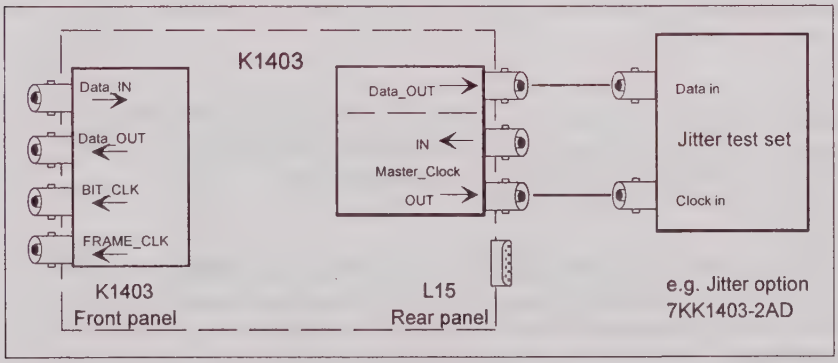


Fig. 3.2: Connection to measurement of jitter amplitude

B. Jittering of transmitted signal

The L15 module can also transmit with the externally set and jittered system clock. In this measurement, the following two sockets are connected to the jitter modulator.

Master_Clock OUT :

This clock is the module-internal system clock. The output has CMOS level. The frequency is 12.288 MHz.

Master_Clock IN :

The clocks at the transmitter end are derived from this clock. The input level may lie between 1 V and 5 V, the frequency is 12.288 MHz as for Master_Clock OUT.

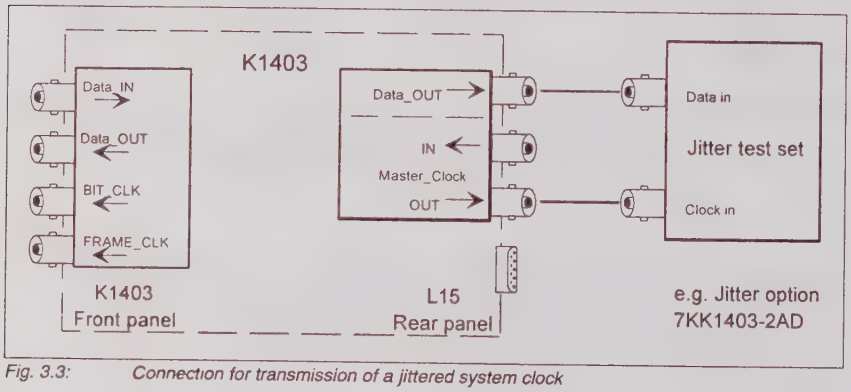


Fig. 3.3: Connection for transmission of a jittered system clock

C. S_0 bus monitor

The S_0 bus data at the receiver end can be displayed and analyzed on an oscilloscope.

Data OUT :

The electrically isolated and amplified S_0 bus signal is provided here. The amplitude is amplified up to 4.7 times depending on the S_0 bus level at the receiver end and has an amplitude of approx. 1 V. The S_0 bus bit rate is 192 kHz.

FRAME_CLK :

This clock is the frame clock of the S_0 signal whose frequency is 4 kHz, 8 kHz, 16 kHz or 32 kHz. The frame clock is synchronous with the received signal. The rising edge of this clock at 4 kHz has the same timing as the rising edge of the F bit of the S_0 received signal.

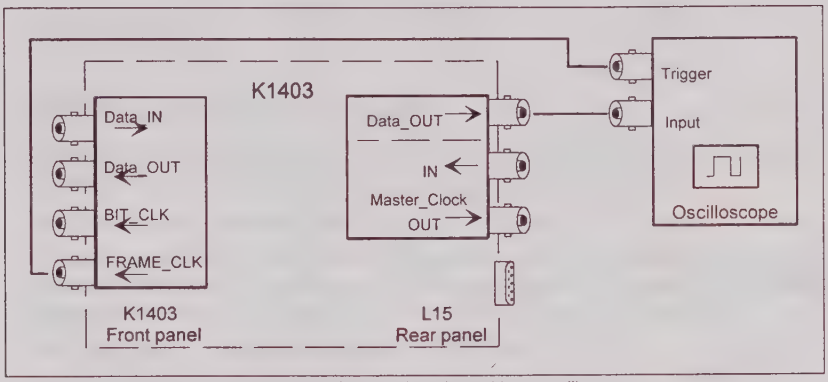


Fig. 3.4: Connection for analysis of the S_0 bus data with an oscilloscope

D. Connection of a data terminal

The processor used for communication of layers 2 and 3 can be controlled via the external V.24 socket. The data can be sent manually and indicated by scanning on the terminal. This mode is reserved for testing and for later applications and is not accessible to the user.

The data terminal must be set as follows:

Baud Rate : 9600

Data Bit : 8

Stop Bit : 1

Parity : off

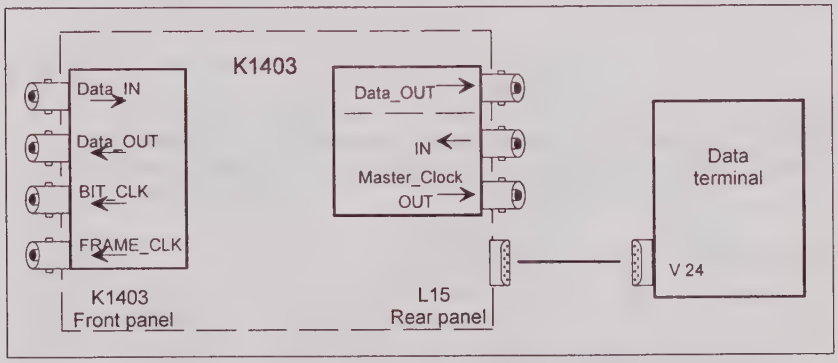


Fig. 3.5: Connection for control of the layer 2/layer 3 processor via a data terminal

E. External data coupling-in/out

Data can be coupled-in into the required data channels on the S_0 bus or coupled-out from the channels using an external data source/sink. All inputs and outputs have CMOS level.

The received data of the K1403 at the socket "Data IN" is transferred on the L15 module by the falling edge of "BIT CLK". Otherwise the rising edges of "FRAME CLK", "BIT CLK" and "Data OUT" have the same timing.

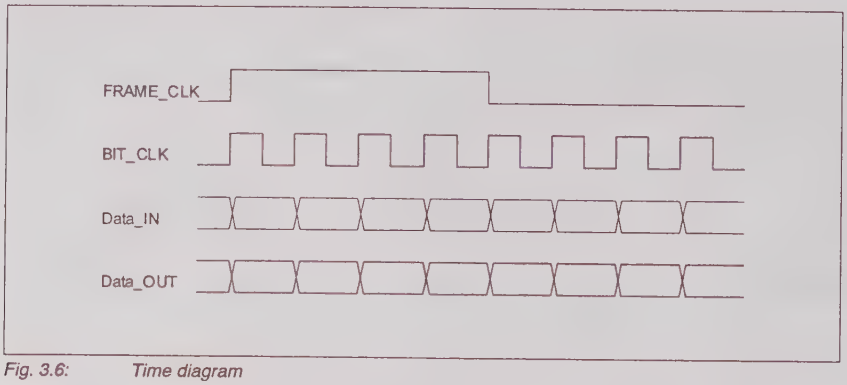


Fig. 3.6: Time diagram

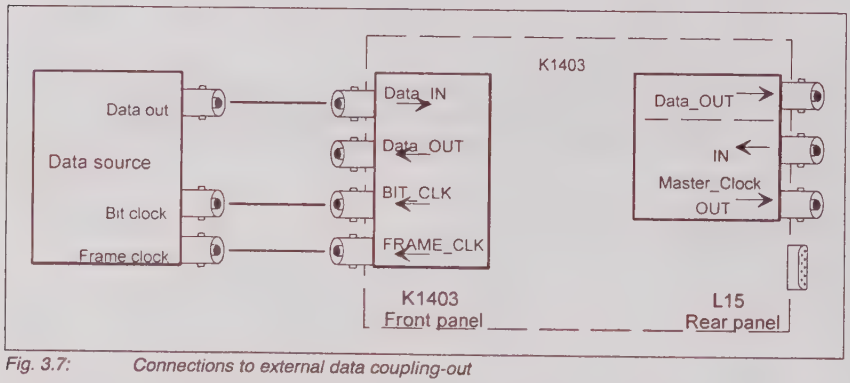


Fig. 3.7: Connections to external data coupling-out

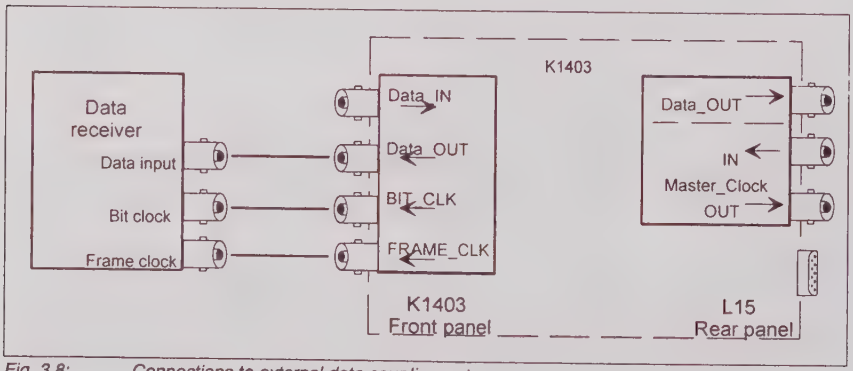


Fig. 3.8: Connections to external data coupling-out

4 Operation

4.1 Control elements and sockets

The functional tests module can be supplied with an additional software with which all TTCN tests according to CTS-2 Appendix B2 can also be executed.

It is available under order no. 7KK1403-6AC10.

After switching on the unit and initialization of the functional tests module, the module registers with its hardware and software version numbers. The following lines appear in the display in addition to the other configuration messages:

FUNCT(1) : SW : V4.00 HW: 2.0 DATE TIME B1

FUNCT(2) : SW : V4.00 HW: 1.1 DATE TIME B2

SW: V4.00: Software version number of processor for layer 1

SW: V4.00: Software version number of processor for layer 2/3

HW: 2.0: Hardware version number of module

Date /Time: Date and time of manufacture of the software available on the module

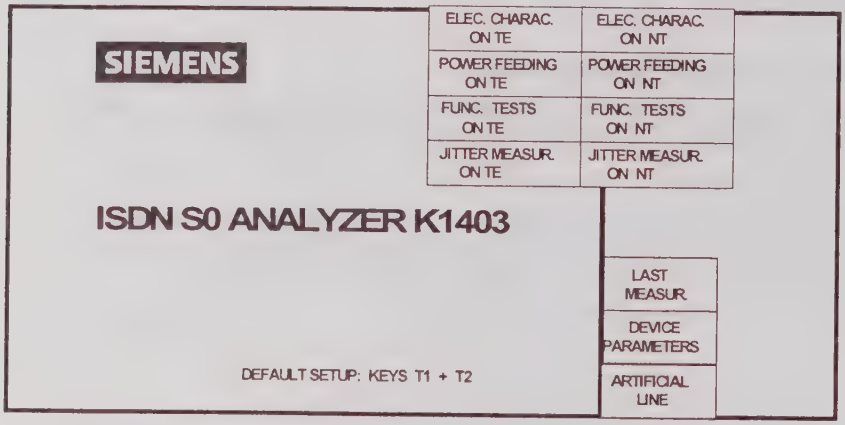
B2: appears at the end of the funct(2) string if the module is equipped with the additional software for the tests according CTS-2 Appendix B2.

The indicated versions may have a different state as a result of product updating.

The measuring mode Receiver sensitivity implemented on this circuit board for technical reasons is present in the menu ELECTRICAL CHARACTERISTICS TESTS ON TE/NT.

Initial program loading of the unit must be carried out when switching it on for the first time after installing the option. To do this, press keys T1 and T2 simultaneously. This is not necessary if the option has already been fitted in the factory.

The basic menu appears in the display following the initialization phase.



To call up the functional tests on the TE or NT press

`FUNCT. TESTS ON TE`

`FUNCT. TESTS ON NT`

The following abbreviations are used in the description below:

Abbreviation	**Meaning**
AMI	Alternate Mark Inversion
CCITT	International Telegraph and Telephone Consultative Committee
CTS	Conformance Test Standard
CTS-2-ISDN	This document was produced by the "*CTS-2-ISDN Basic Access Layer 1 sub-working group*". It is based on the European Telecommunications Standard ETS 300 012 and on the CCITT recommendation I.430 (blue book).
PICS	Protocol Implementation Statement
PIXIT	Protocol Implementation Extra Information for Testing
PRBS	Pseudo Random Binary Sequence
TEI	Terminal Endpoint Identifier
TTCN	Tree and Tabular Combined Notation (s. ISO/IEC IS-9646-3)

5 Measurement and presentation of results

5.1 Functional Tests TE

It is recommended to carry out one of the two measuring modes

- Basic interconnection test on TE,
- binary organization of frame on TE

before carrying out the TTCN tests described in Sections 4.2.3 or 4.2.4. The test object is activated completely in these tests if this is possible. The optimum setting of the adaptive input amplifier of the module is carried out in the process. The setting established for this test setup is also retained for the TTCN tests.

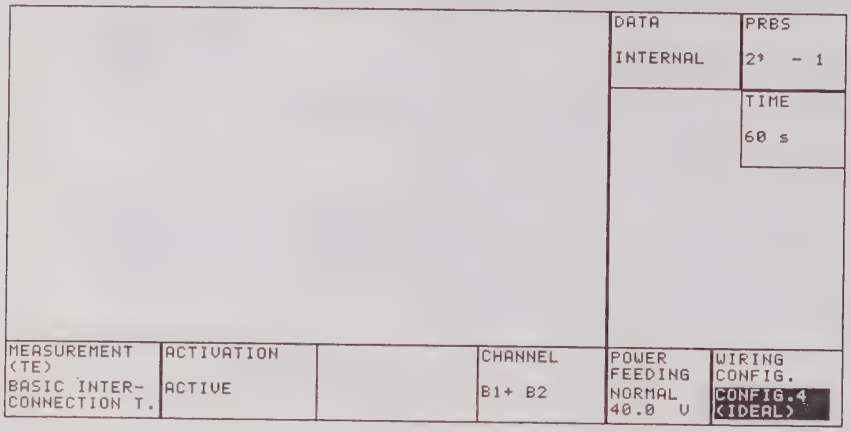
The S_0 terminal resistors have a fixed setting of 50Ω. A selection between 50Ω and 100Ω is only possible in combination with the artificial line in the measuring mode Basic interconnection test on TE.

All functional tests are divided into four measuring modes:

- Basic interconnection test
- Binary organization of frame
- TTCN tests according to CTS-2 Appendix
- TTCN tests according to CTS-2 Appendix

The tests defined in TTCN include a large number of different test sequences which are summarized in test groups (TEST MODE) of 6 for CTS-2 Appendix B1 or 2 for CTS-2 Appendix B2 respectively.

5.1.1 Basic Interconnection Tests



Setting parameters (MENU)

MEASUREMENT (TE)
BASIC INTER-CONNECTION T. ✓
BIN. ORG. OF FRAME
TTCN-TESTS APPENDIX B1
TTCN-TESTS APPENDIX B2

ACTIVATION	CHANNEL	TIME
AKTIVE ✓	B1	EDIT: 5...300 s
PASSIVE	B2	60 s ✓
UPSTREAM	B1 + B2 ✓	
DOWNSTREAM		

PRBS	DATA	POWER FEEDING
2^9 -1 ✓	INTERNAL ✓	NORMAL ✓
2^{11} -1	EXTERNAL	RESTR.
2^{15} -1		EXTERNAL
2^{20} -1		

WIRING-CONFIG.	P.NUMBER > SUB.ADR. >	INFORMATION TRANS. CAPAB:
FREE CONFIG.	P.NUMBER	SPEECH
CONFIG. 1	SUB.ADR.	AUDIO 3,1 kHz
CONFIG. 2	CLEAR	DATA
CONFIG. 3a	RETURN	AUDIO 7,0 kHz
CONFIG. 3b		VIDEO
CONFIG. 4 (IDEAL)		

Only with additional software:

TTCN-TESTS APPENDIX B2

The *line configuration* is realized with the option **ARTIFICIAL LINE**.

ARTIFICIAL LINE OPTION

Dependencies

POWER FEEDING		
NORMAL	RESTRICTED	EXTERNAL
EDIT	EDIT	-
40V	40V	-

DATA	
INTERNAL	EXTERNAL
PRBS	---
2^9-1	---
2^{11}-1	---
2^{15}-1	---
2^{20}-1	---

ACTIVATION			
UPSTREAM / DOWNSTREAM		ACTIVE / PASSIVE	
P.NUMMER > SUB.ADR. >	TIME *)	P.NUMBER > SUB.ADRESS > *)	TIME
P.NUMBER	---	---	EDIT: 5...300s
SUB.ADR.	---	---	60 s
CLEAR		---	
RETURN		---	

*) not displayed

Test description

In this test described in CTS-2-ISDN Basic Access § D1, the ability of the test object to carry out elementary layer 1 procedures is checked, e.g. whether it can transmit INFO3 if INFO2 has been received. This test is the first one to be carried out since, as the name indicates, the execution of further tests is either not possible or not technically meaningful in the case of a non-conformal test object. In addition, the bit transparency is tested for one minute with a PRBS pattern. The terminal equipment must be able to switch a suitable data loop for B1, B2 or B1+B2 in a test mode.

If the data coupling-in is switched to EXTERNAL, the values bit error (BE) and bit error rate (BER) remain at zero and the conformance result is set to INCONCLUSIVE, as the measurement of the Bit error rate has to be carried out externally.

"Basic interconnection tests" on TE should be carried out with all defined CCITT line configurations. To start the measurement press

`START/STOP`

The conformance test is carried out with the following parameter settings:

Activation	: aktive and passive
Channel selection	: B1, B2
Data	: Internal, PRBS 2^9 -1
Power feeding	: Normal, 40V
Line config.	: CCITT configuration I, II, IIIa, IIIb and IV each with and without 200-kHz and 2-MHz interferences

The following error or status messages may occur:

Message	Comment
FKT : no INFO0 det.	No INFO0 has been received (possible with deactivation test)
FKT : no INFO1 det.	No INFO1 has been received.
FKT : no INFO3 det.	No INFO3 has been received.
FKT : INFO0 det.	INFO0 has been received.
FKT : undef. INFO !	No defined INFO has been received.
FKT : USER CALL	Outgoing call. Pick up phone!
FKT : wrong Amplitude	Receiver amplitude too large or too small.
MEASUREM. finished	Measurement finished.

Basic interconnection test in layer 3

In the measurement mode basic interconncection tests of the SW version V4.0, you can also activate a basic interconnection test (ongoing communication) in layer 2 and 3 apart from the activation of layer 1. Herefore, the K1403 simulates the necessary parts of the network protocol which was based on the EDSS1 protocol.

The setting of the necessary parameters is implemented via the following control keys:

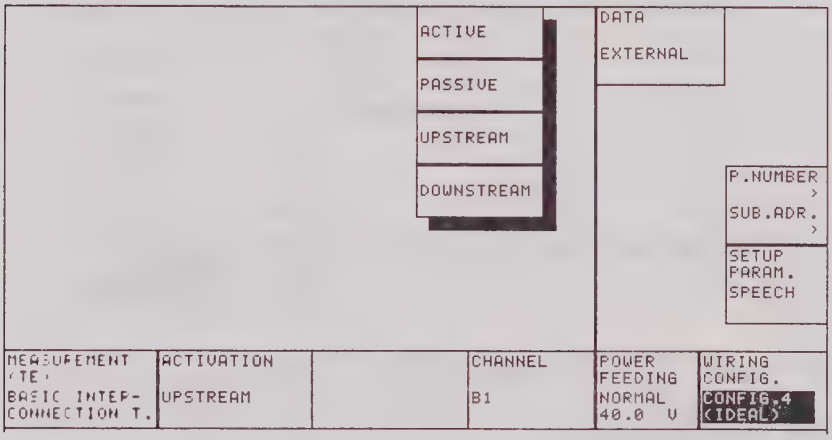
Activation

Mode

Channel selection

P. Number & Sub. Adr.

Information transmission capability



ACTIVATION

You can either select the activation of layer 1 or also the complete activation of layer 1, 2 and 3:

- ACTIVE
- PASSIVE
- UPSTREAM
- DOWNSTREAM

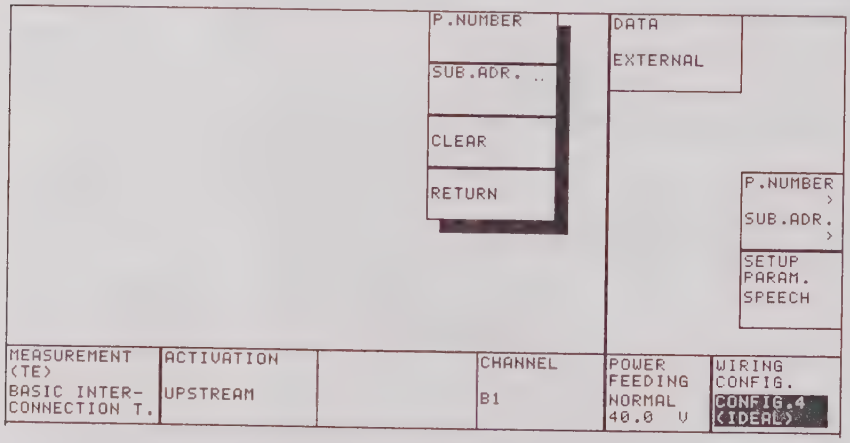
In case of PASSIVE and UPSTREAM, the K1403 waits for a basic interconnection test initiated by the TE, in case of ACTIVE and DOWNSTREAM the K1403 activates on its own.

Channel

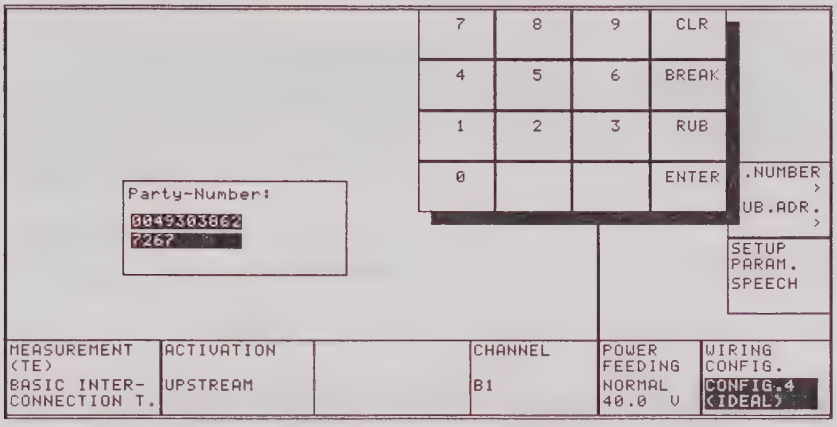
With this parameter you select the B-channel to be determined (B1 or B2). This channel can be connected to the BU2-BU5 sockets and thus it is available there for the connection to an external data source/sink. If the complete activation of layer 1, 2 and 3 is selected, there is no selection possibility for B1+B2 .

To the B-IN, B-OUT, CLK and FSC sockets e.g. a half-channel test set such as the SIEMENS P2112 can be connected. With this it is possible to carry out analog measurements at an ISDN telephone (CODEC tests).

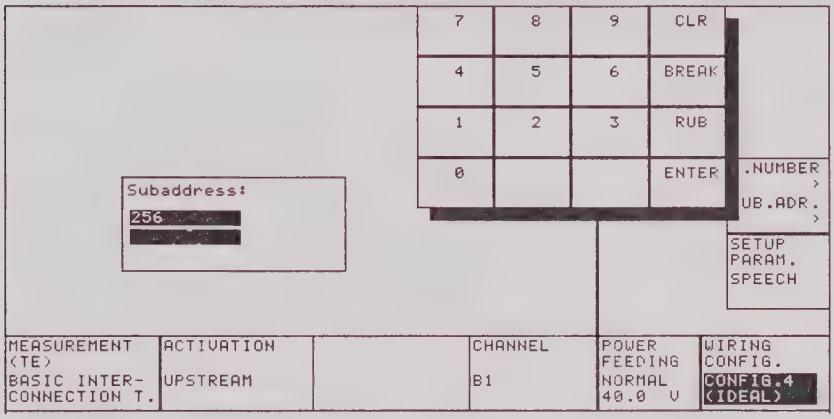
P.NUMBER / SUB.ADR.



With this key you are given the possibility for an input of a 20-digit call number (Called Party Number) and a 20-digit extension number (Called Party Subaddress). The input is carried out via an editing window. With the RETURN key, you leave the input window.



After touching the field `P. Number` you get the editing field for a 20-digit call number. Enter the desired value and terminate this procedure with ENTER.



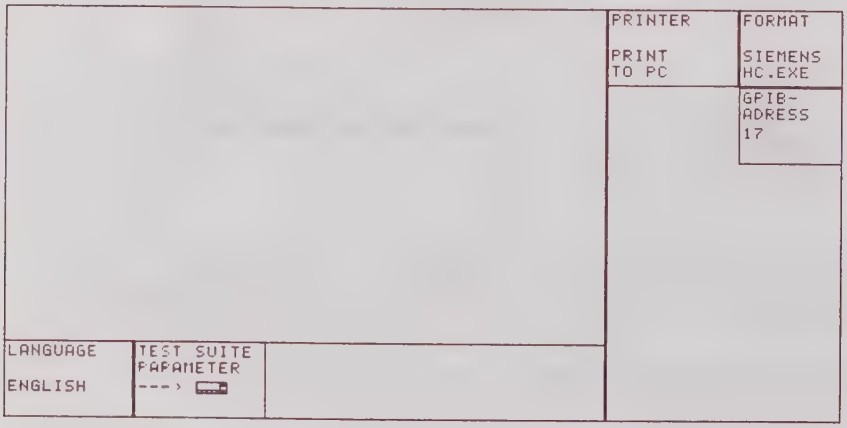
If you have pressed the SUB.ADR. key, you can enter a 20-digit number with which a specific terminal at a private branch network can be selected.

Information transmission capability

An element of the SETUP message, with which the basic interconnection test of layer 3 is initiated, is the information transmission capability (Bearer Capability). With this parameter the service is determined on which the connection shall be based. The following selection can be made.

- Speech
- AUDIO 3.1kHz
- Data
- AUDIO 7.0kHz
- Video

The establishment of a connection (ongoing communication) in layer 2 and 3 depends on the characteristics of the test object. These characteristics are defined as PICS/PIXIT variables in the "CTS-2-ISDN Basic Access" manual and for a correct test sequence they ***must*** be set ***prior to the start***. In contrast to previous software versions, version 4.0 now also allows that these variables, which will be referred to as **"TEST SUITE PARAMETERS"**, can be set in the DEVICE PARAMETER MENU.



Procedure

After the measurement was started with the START key, the K1403 asks the user to initiate a connection (<USER CALL>), if the parameter ACTIVATION was set to PASSIVE or UPSTREAM, or it is necessary to accept the call, i.e. to acknowledge the connection if the parameter ACTIVATION was set to ACTIVE or DOWNSTREAM.

Presentation of results

The results are displayed in the following form:

BE :	Count		Count of bit error counter; max 2^{32}
TIME:	Count	s	Count of expired seconds; max. 2^{32}
BER:	Bit error rate	BE/s	Continuously calculated bit error rate
Conformance	TRUE/FALSE/INC.		not used
ACTIVATION:	TRUE/FALSE		Result of Layer 1 activation
DEACTIVATION	FALSE		not used

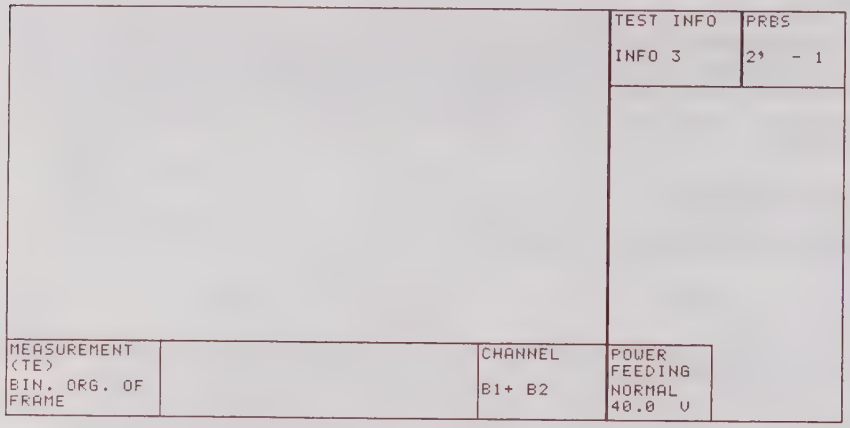
The bit error measurement is only active with an internal data source.

The following additional error or status messages may result:

Message	Comment
FKT : L3 established	if a complete layer-3-connection was established
FKT : no L3 connect.	layer 3 connection not possible
MEASUREM. aborted	Measurement aborted

The measurements with a connection (ongoing communication) in layer 2 and 3 are automatically carried out as continuous measurement. The length of the measurement time is determined by the user. The measurement is terminated with the START/STOP key.

5.1.2 Binary Organization of Frame



Setting parameters (MENU)

MEASUREMENT (TE)
BASIC INTER-CONNECTION T.
BIN. ORG. OF FRAME
TTCN-TESTS APPENDIX B1
TTCN-TESTS APPENDIX B2

TEST INFO	CHANNEL	PRBS	POWER FEEDING
INFO 3	B1	2^9 -1	NORMAL
INFO 1	B2	2^{11} -1	RESTR.
	B1 + B2	2^{15} -1	EXTERNAL
	B1 + B2 + D	2^{20} -1	

Only with additional software

TTCN-TESTS APPENDIX B2

Dependencies

POWER FEEDING		
NORMAL	RESTRICTED	EXTERNAL
EDIT	EDIT	-
40V	40V	-

TEST INFO		
INFO 3		INFO 1
PRBS	CHANNEL	---
2^9-1	B1	---
2^{11}-1	B2	---
2^{15}-1	B1 + B2	---
2^{20}-1	B1 + B2 + D	---

Test description

Test A (A.5.4.2.1, A5.5, A5.6-ETS300 012)

Test B (A.6.2.2-ETS300 012)

In this test described in CTS-2-ISDN Basic Access § D2.1.1 and §D2.1.2, the frame structure of the INFO1 and INFO3 signals is tested. The signals are transmitted on the S_0 bus with the DC-free AMI code. This signal, consisting of 3 levels (+Unom, 0, -Unom), should satisfy certain criteria in a 48-bit S_0 frame. In addition to generation of the double code violation, these criteria also include the ternary setting of the level in the B-channels. This is stimulated by transmitting a PRBS signal in the B-channels. The received bits of an S_0 frame with its AMI level are displayed in envelope mode. A data loop must be switched in the test object in order to test the B-channels.

To start measurement press

START/STOP

If no valid information is detected, the S_0 data is presented as a single shot and not in envelope mode. The S_0 data on the receiver end is thus visible for the user (oscilloscope function).

The conformance test is carried out with the following parameter settings:

a)

Test INFO : INFO 3

Channel selection : B1 + B2 + D

PRBS : 2^9 - 1

Power feeding : Normal, 40V

Result : Graphic

b)

Test INFO : INFO 1

Power feeding : Normal, 40V

Result : Graphic

The results for various INFO3 and INFO1 frames are displayed below. The asterisk for each bit position means that not all possible levels have been detected (envelope mode). The legend indicates the significance of the 48 bits of a frame. Only the bit pattern is displayed for INFO1.

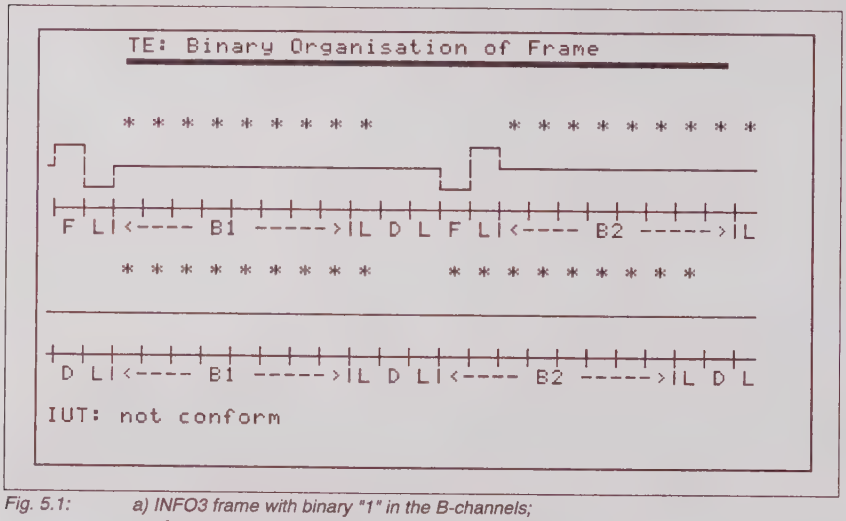


Fig. 5.1: *a) INFO3 frame with binary "1" in the B-channels;*
conformance test for B1+B2;
Result does not conform since not all possible levels were detected.

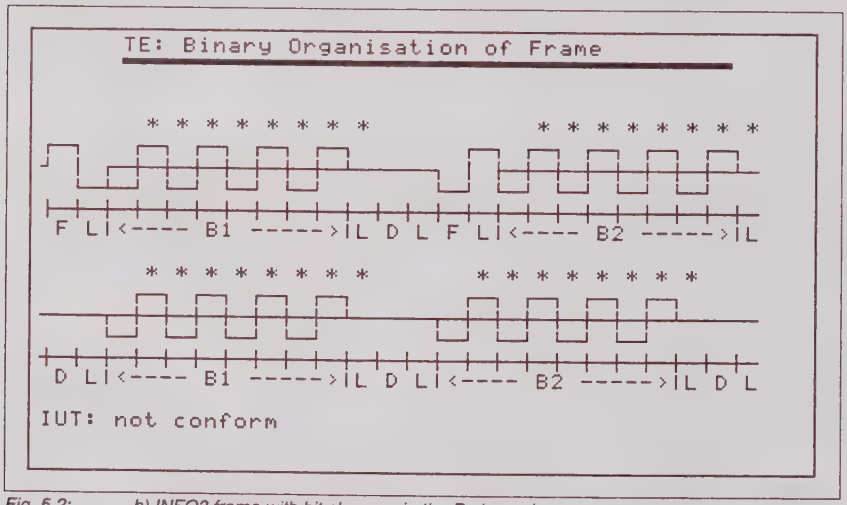


Fig. 5.2: *b) INFO3 frame with bit changes in the B-channels;*
conformance test for B1+B2;
Result does not conform since not all possible levels were detected.

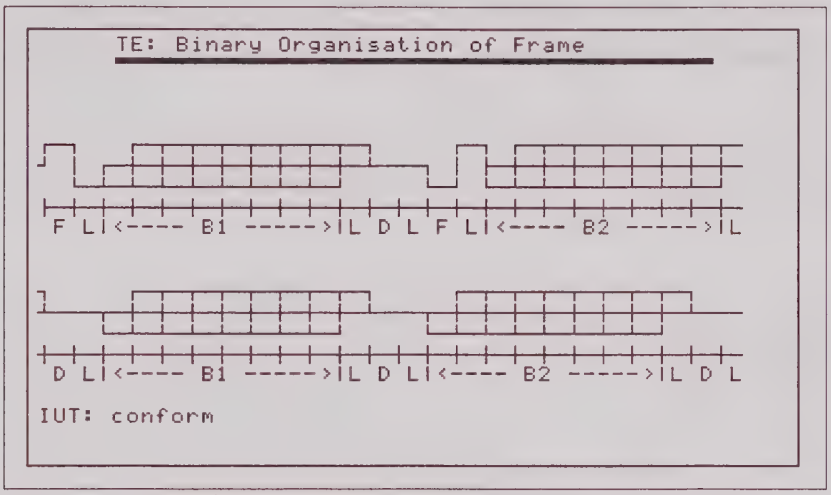


Fig. 5.3: *c) INFO3 frame with all possible bit changes (PRBS pattern) in the B-channels; conformance test for B1+B2; Result conforms since all possible levels were detected.*

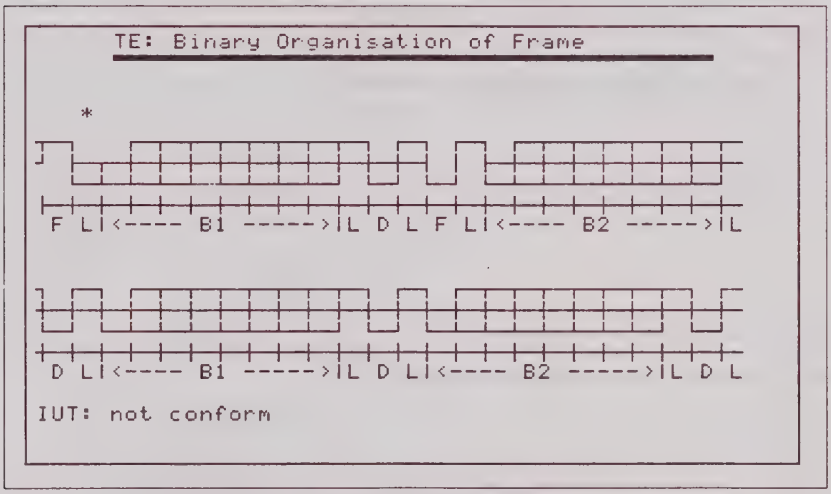


Fig. 5.4: *d) INFO3 frame with all possible bit changes (PRBS pattern) in the B-channels and the D-channel, and one error in the L-bit; conformance test for B1+B2+D; Result does not conform since a biterror was detected.*

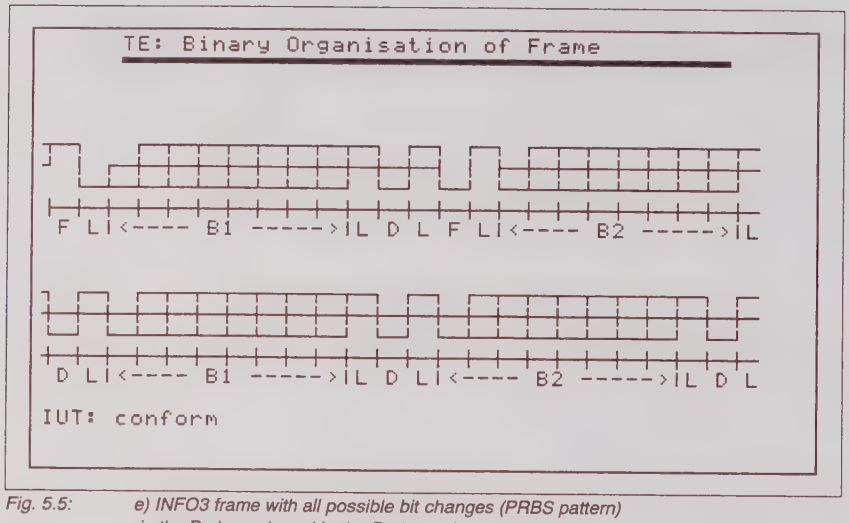


Fig. 5.5: *e) INFO3 frame with all possible bit changes (PRBS pattern) in the B-channels and in the D-channel; conformance test for B1+B2+D; Result conforms since all possible levels were detected.*

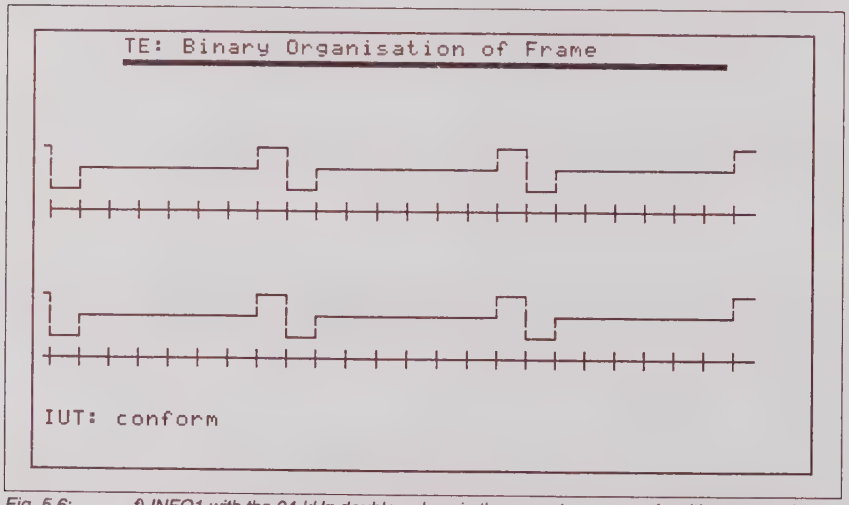
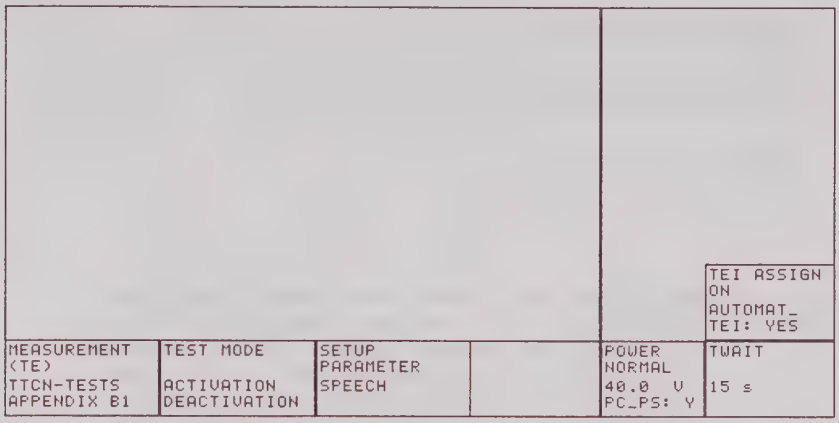


Fig. 5.6: *f) INFO1 with the 24-kHz double pulses in the correct sequence {positive ⇒negative⇒ zero}-level; conformance test for INFO1; Result conforms since all possible levels were detected.*

5.1.3 TTCN - Tests (Appendix B1)



Setting parameters (MENU)

MEASUREMENT (TE)
BASIC INTER-CONNECTION T.
BIN. ORG. OF FRAME
TTCN-TESTS APPENDIX B1
TTCN-TESTS APPENDIX B2

TEST MODE	INFORM. TRANS. CAPABILITY
D-CHANNEL ACCESS CONTR.	SPEECH
ACTIVATION DEACTIVATION	AUDIO 3,1 kHz
TIMERS FOR ACTIVATION	DATA
FRAME ALIGNMENT	AUDIO 7,0 kHz
MULTI-FRAMING	VIDEO
B-CHANNEL CONTENT	

TEST SUITE PARAMETER	TWAIT
MENU DISPLAY	EDIT: 0...250s

TEI ASSIGN
ON
OFF
EX-TERNAL

POWER FEEDING
NORMAL
RESTRICTED
EXTERNAL

Only with additional software

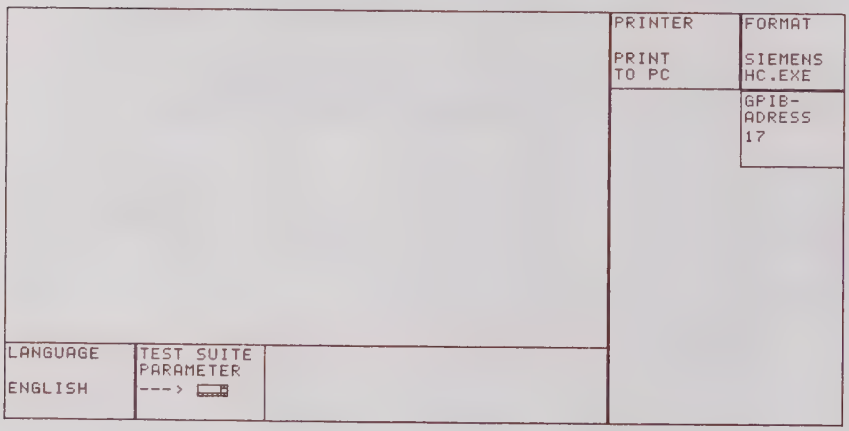
TTCN-TESTS APPENDIX B2

Dependencies

The following dependencies are available in this menu:

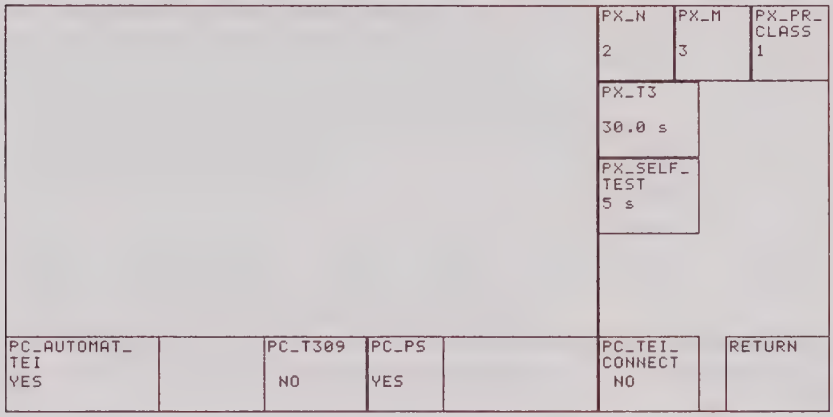
POWER FEEDING		
NORMAL	RESTRICTED	EXTERNAL
EDIT	EDIT	-
40V	40V	-

The establishment of a connection (ongoing communication) in layer 2 and 3 depends on the characteristics of the test object. These characteristics are defined in the CTS-2 ISDN Basic Access Manual as PICS/PIXIT variables and ***must*** be set ***before the start*** of the test defined in TTCN to ensure a correct test sequence. In contrast to previous software versions, version 4.0 now also allows that these variables, which will be referred to as **"TEST SUITE PARAMETERS"**, can be set in the SETUP MENU.



Submenu TEST SUITE PARAMETER

The functional test sequences described in CTS-2 TTCN are dependent on the characteristics of the test object. These characteristics are defined in the CTS-2 ISDN Basic Access Manual as PICS/PIXIT variables and ***must*** be set ***before the start*** of the test defined in TTCN to ensure a correct test sequence. These variables will be referred to as "TEST SUITE PARAMETERS".



Setting parameters (MENU)

MEASUREMENT (TE)
BASIC INTER-CONNECTION T.
BIN. ORG. OF FRAME
TTCN-TESTS APPENDIX B1
TTCN-TESTS APPENDIX B2

TEST SUITE PARAMETER	PC_AUTOMAT_ TEI	PX_N	PX_M	PX_PR_ CLASS	PC_T309
MENU DISPLAY	YES	EDIT: 2...250	EDIT: 3...250	1	YES
	NO			2	NO

PC_PS	PX_T3	PX_SELF_ TEST	PC_TEI_ CONNECT	PC_DE
YES	EDIT: 1...30 s	EDIT: 0....4400 s	NO	YES
NO			YES	NO

Only with additional software

TTCN-TESTS APPENDIX B2

Dependencies

PC_AUTOMAT_TEI	
YES	NO
PC_TEI_CONNECT	-
NO	-
YES	-

PC_PS	
YES	NO
-	PC_DE
-	YES
-	NO

Further dependencies are described in the *Parameter description of the measuring mode TTCN-Tests Appendix B1-TE* of the operating manual of the K1403 **C73000-B6000-C153**.

Parameter description

The variables and their PICS/PIXIT numbers are described in the table below.

Name	Type	PICS/ PIXIT	Comment
PC_AUTOMAT_TEI	B	L6/3	TE with automatic TEI-assignment;
PC_TEI_CONNECT	B		TEI={64...127}
			TE requires TEI assignment directly after
PC_T309	B	N6/7	connection to an NT (mains)
PC_PS	B	P1/2	TE with implemented timer T309
		P1/3	Supply via S0-Bus (PS1 or PS2)
		P1/8	
PC_DE	B	P1/1	
		P1/9	TE with voltage detector (only for terminal
		P1/10	equipment which is not supplied via the S_0
PX_N	N	PX2/3	bus)
PX_M	N	PX2/4	Number of "bad" S_0 frames required to achieve Frame loss
PX_T3	V	PX2/1	Number of "good" S_0 frames required to achieve Frame alignment again
PX_PR_CLASS	N	PX2/6	Value of T3 timer
PX_SELF_TEST	V	PX2/5	Priority class of the terminal equipment
			Self-test time of terminal equipment

In the column **Type**, the letter **B** stands for a Boolean variable, **N** for a natural number and **V** for an adjustable value.

There are three independent and two dependent Boolean variables. If "PC-AUTOMAT-TEI" is set to "no", setting the variable "PC-TEI-CONNECT" is not required. Similarly it is not necessary to set "PC-DE" if "PC-PS" is set to "yes" (TE with voltage supply via the S_0 bus). The dependent parameters are enabled in the menu only if it is practical to set them.

Depending on these TEST SUITE PARAMETERS which describe the various characteristics of a TE, the CTS-2 guidelines define various tests according to the version of the test object and omit those tests whose execution would not be useful. Among the test groups of the functional tests only those tests are offered for selection in the menu which will be used to test the terminal device according to the CTS-2 guidelines due to its special characteristics. All TEST SUITE PARAMETERS set here will be transferred during the test sequence itself (e.g. running time of the various timers, required number of specific S_0-frames, etc.)

Setting the TEST SUITE PARAMETERS is absolutely required for the execution of the functional tests according to CTS-2 Appendix B1 and Appendix B2 in TTCN; with the exception of the UPSTREAM / DOWNSTREAM basic interconnection test, these settings have no meaning for the measurements with the K1403!

After setting the TEST SUITE PARAMETERS, you can return to the functional tests main menu by pressing

ETURN

In addition to the various settings of the TEST SUITE PARAMETERS which adapt the test sequences to the test object as described above, some parameters of the test sequence are freely selectable. In the following, these parameters will be referred to as MEASUREMENT PARAMETERS.

The following MEASUREMENT PARAMETERS can be set:

Name	Settings	Comment
SETUP PARAMETER	Speech Audio 3,1 kHz Data Audio 7,0 kHz Video	Part of the Bearer Capability Information Element according to ETS 300 102-1, describes the type of service used. (only for important tests which require a layer 3 Basic interconnection.) 1)
POWER FEEDING	normal restricted external	Supply voltage to be set as described above.
TWAIT	0 ... 250 s	Waiting time during the test sequence in which an operator input at the test object is required (e.g. after the prompt "User Call").
TEI ASSIGNMENT	on off	Determines whether the tests on TEs with automatic TEI assignment are to take place with or without assigned TEI. 2)

1)

In the case of tests from Appendix B1, this applies only to the following Timer tests: **TIF7compdeact1, TIF7compdeact2, TIF8compdeact1, TIF8compdeact2.**

2)

In the case of tests from Appendix B1, this applies only to the following D-channel access tests: **DCPriorityClass1, DCPriorityClass2, DCNormtoLowPLCL1, DCNormtoLowPLCL2, DCLowtoNormPLCL1, DCLowtoNormPLCL2.**

The MEASUREMENT PARAMETERS are integrated in the main menu of the functional tests defined in TTCN. They are described together with the setting parameters of the menus of the TTCN-Tests Appendix B1.

In order to start the functional tests defined according to CTS-2 Appendix B1 in TTCN, select one ot the test groups described below (see Section 4.2.3.1 to 4.2.3.6) by pressing

`TEST MODE`

To activate the selected **TEST GROUP** press

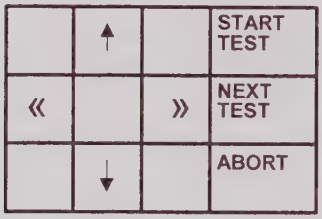
`START/STOP`

The TEST SUITE PARAMETERS set previously are evaluated, and a selection of tests suitable for the connected test object appears in the main window of the K1403 display.

The START/STOP key only activates a selection process and does not yet start a test sequence!

All tests displayed are appropriate for the test object connected according to the CTS-2 definition. Due to limited space the names of the individual tests are displayed in abbreviated form. A cursor (inverted characters) marks the test selected and its full name according to CTS-2 is displayed directly above the selection window.

In addition, the following softkey pad is displayed to the right of the main window:



Using these softkeys the selection process of the tests as well as the test sequence can be controlled. The cursor can be moved to the abbreviated name of the desired test using the cursor softkeys. The functional tests main menu continues to be displayed for information about the settings that have already been made, but it is not available for operation.

To start the actual test sequence press the softkey on the display:

START/TEST

The K1403 now executes the selected test according to the test scenarios defined as TTCN tables in the CTS-2.

If during the test sequence a manual operator input on the test object is required, messages are output on the display of the K1403 in a message window.

Messages	Description
FKT: USER CALL	User prompt to activate the S_0-interface via the test object (e.g. pick up telephone receiver).
FKT: USER CALL AGAIN	Second user prompt for activation.
FKT: USER DISCONNECT	User prompt to interrupt an existing connection via the test object (e.g. put down telephone receiver).

If a Basic interconnection is set up over the network during the test sequence, a manual input is required after the corresponding call signal on those test objects which do not react automatically to Basic interconnection (e.g. pick up telephone receiver).

If a test sequence requires **switching the supply voltage** of the test object, the switching operation ***must*** be **controlled via the K1403**. If a phantom-powered TE is tested (TEST SUITE PARAMETER "PC-PS" = yes), this condition is fulfilled because the K1403 itself supplies the phantom power and can switch the supply voltage of the TE depending on the test scenarios. If, however, a **locally supplied**

TE is connected to the K1403 as measurement object, this TE must be connected to a supply voltage via an **external switching element** (relay). For control of this external switching element via the K1403, a switching voltage is available at the module for **power feeding (C73249-A11-L100)**.

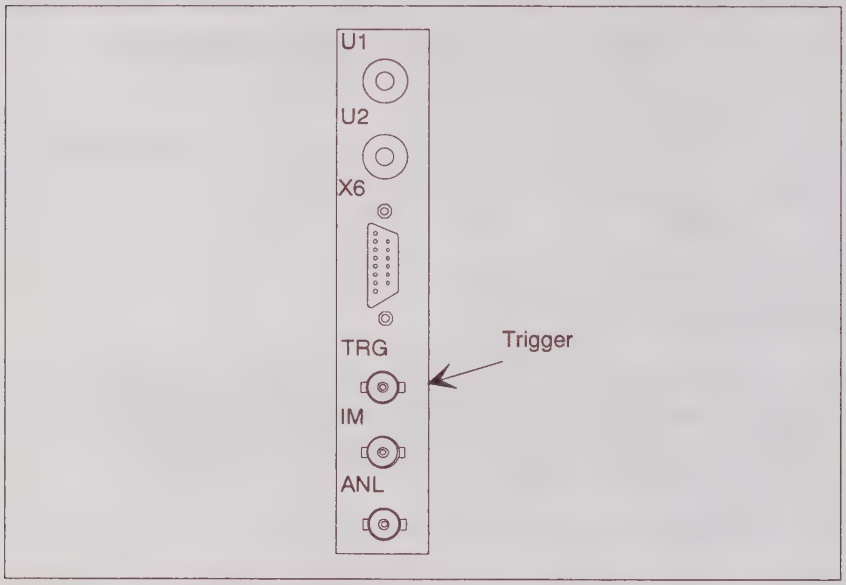


Fig. 5.7: Connections of power feeding module

The above figure shows the module as it is seen from the rear of the K1403. The switching voltage is available at the terminal "TRG"; a locally supplied TE is to be switched on with +5 V and switched off with 0V. Below follows a possible realization of the external switching element.

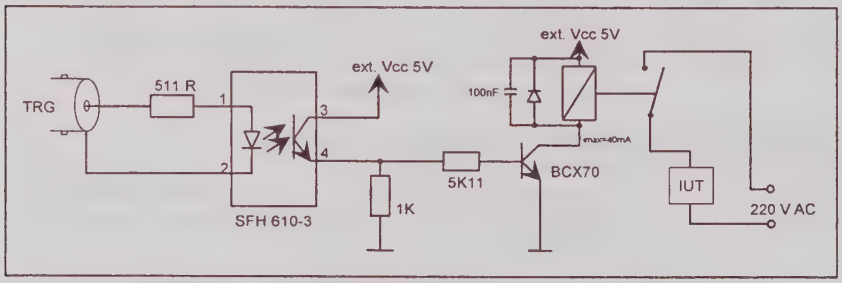


Fig. 5.8: Switching the local power supply of a TE through the K1403

Each test is completed automatically. The test results are entered on the display of the K1403 to the right of the abbreviated test name. There are three different test results (verdicts):

P : passed /

F : failed /

I : inconclusive / repeat test!

The selected test can be repeated any number of times. If different results are reached for the same test, they are displayed next to each other. The result of the last test executed is displayed additionally in the lower right corner of the main window for easy identification.

Only the results of the test sequences are displayed on the K1403!

If you need further information about the test sequence or if the results obtained by the K1403 need to be logged in a protocol, we recommend the following software tools:

1. PC Trace Analyzer for all tests defined in TTCN

(order no. 7KK1403-6AB11)

This program operates on a PC connected via one of its serial interfaces to the V.24 terminal of the functional tests module. During the test whose TTCN definition usually consists of many different TTCN tables, the completion of each individual TTCN table is displayed in real time on the screen of the PC. Thus the status of the currently running test is always known during the entire test sequence. This is especially advantageous when running long tests. After completion of a test, the functional tests module outputs up to 256 code numbers (trace) to the PC. With the aid of these numbers, a clear analysis of the test sequence is possible. The trace analyzer program displays all tables of the relevant test in a form almost identical to CTS-2; those lines that the test has already passed are marked in color. All traces recorded can be saved as files on the PC for later analyses.

2. Remote Control PC Software for the K1403

(order no. 7KK1403-6AA11)

This software package allows comfortable automation and linking of measurement sequences of the K1403. The linking of different tests is ideally suited for the functional tests defined in TTCN, especially if all tests of one test group are to be executed. The software operates on a WINDOWS interface so that all results obtained with the K1403 can be directly incorporated into the different word processing programs operating under WINDOWS (e.g. WORD for WINDOWS). Thus it becomes very simple to create test documents on ISDN terminal devices to be tested. In the case of the functional tests defined in TTCN, the results as well as the trace sequences can be entered in the documents. Additionally, files are created with which the various tests can be thoroughly analyzed later using the **PC Trace Analyzer** mentioned above.

To start the test following the one selected with the cursor in the selection list touch

NEXT TEST

Thus, several tests listed one after the other in the selection list can easily be executed in succession without using the cursor keys. This method is especially suitable if **all** tests of a test group are to be carried out.

Any running test can be aborted before its automatic completion by pressing

ABORT

Instead of a test result, the letter "**B**" (BREAK) is entered next to the abbreviated test name. This "**B**" disappears if the same test is completed normally after a restart.

The active status of the current test group is ended by pressing the key

START/STOP

The softkey pad for test selection then is deleted from the display, while the results of all tests executed in the test group are retained in the main window. This results display can be saved using the MEMORY menu of the K1403. The functional tests main menu is now enabled again, and another test group can be selected, for instance via the menu TEST MODE.

The different test groups are described below.

5.1.4 D-Channel Access Control Procedure

(§ A.6.1 - ETS 300 012)

Two different types of D-channel access procedures are defined according to CTS-2:

a) *Interframe time fill* (§ A.6.1.1 - ETS300 012)

Terminal equipment which is already activated (layer 1 status F7) is to transmit only binary "1" in the D-channels. In this test, the data in the D-channels is evaluated within a period of 100 ms.

b) *D-echo channel procedure* (§ A.6.1.3 to A.6.1.6 - ETS300 012)

Access of terminal equipment to the D-channel commences following successful execution of the procedure described for CTS. In addition to the *priority class* of the terminal equipment, the procedure also depends on the preliminary status of its *priority level*. The D-channels are also controlled in such a way that the behavior of the test object is checked at a bus configured with several terminal devices.

The following tests are available:

Test-No.	CTS-2 Name Appendix B1	Comment
1	ISDN1/DC/F7/DCBinaryOneCL1	"Interframe time fill" Test for TEs with priority class 1
2	ISDN1/DC/F7/DCBinaryOneCL2	"Interframe time fill" Test for TEs with priority class 2
3	ISDN1/DC/F7/DCNormalPL1CL1	D-channel conflict test: D="1" & E="0" for TEs with priority class 1, normal prior. level
4	ISDN1/DC/F7/DCNormalPL1CL2	D-channel conflict test: D="1" & E="0" for TEs with priority class 2, normal prior. level
5	ISDN1/DC/F7/DCNormalPL0CL1	D-channel conflict test: D="0" & E="1" for TEs with priority class 1, normal prior. level
6	ISDN1/DC/F7/DCNormalPL0CL2	D-channel conflict test: D="0" & E="1" for TEs with priority class 2, normal prior. level
7	ISDN1/DC/F7/DCPriorityClass1	Test of first priority class
8	ISDN1/DC/F7/DCPriorityClass2	Test of second priority class
9	ISDN1/DC/F7/DCNormtoLowPLCL1	Test of priority level change from normal to low for TEs with priority class 1
10	ISDN1/DC/F7/DCNormtoLowPLCL2	Test of priority level change from normal to low for TEs with priority class 2
11	ISDN1/DC/F7/DCLowtoNormPLCL1	Test of priority level change from low to normal for TEs with priority class 1
12	ISDN1/DC/F7/DCLowtoNormPLCL2	Test of priority level change from low to normal for TEs with priority class 2

The tests of this test group are selected as follows:

Measuring mode (TE):

```
TTCN-TESTS APPENDIX B1
```

Test mode:

```
D-CHANNEL ACCESS CONTROL
```

To activate the test group press

```
START/STOP
```

In the main window of the display, all required tests in dependency of the TEST SUITE PARAMETERS "PX_PR_CLASS" appear.

If, for instance, "PX_PR_CLASS = 1", the following display appears on the screen of the K1403:

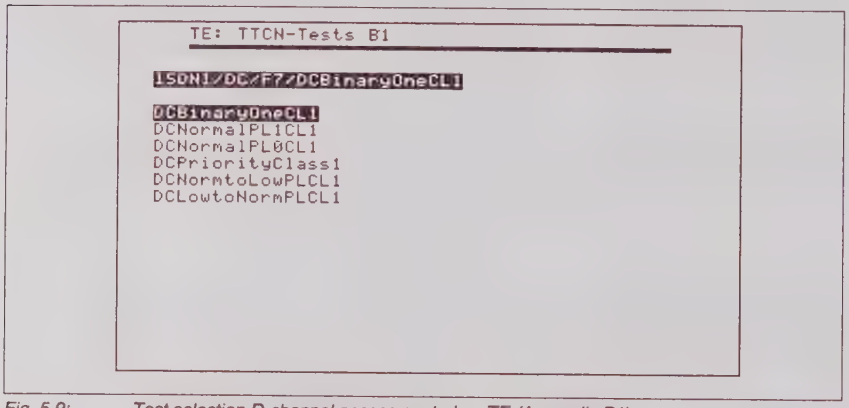


Fig. 5.9: Test selection D-channel access control on TE (Appendix B1)

The tests can now be selected for a test sequence and started as described in Section 5.1.3. After completion of several tests, the following display is possible:

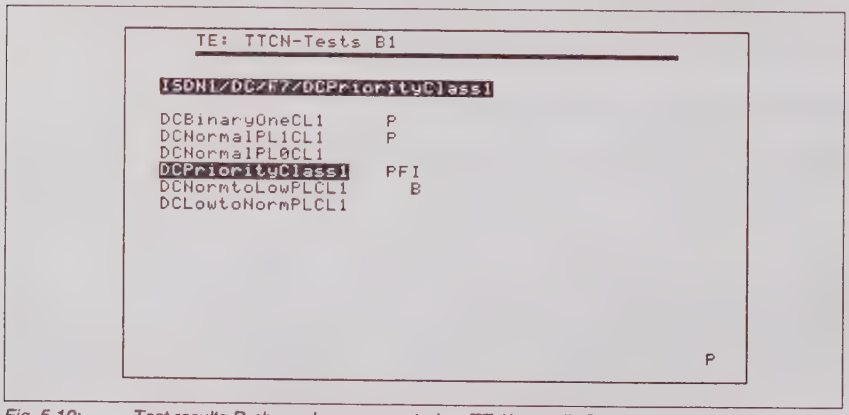


Fig. 5.10: Test results D-channel access control on TE (Appendix B1)

The last test selected is "DCPriorityClass1". It was run at least three times, once each with the results (verdicts) "passed, "failed" and "inconclusive". The letter "P" in the lower right corner of the display shows that the last test run was completed with the result "passed". Before the runs of the last test selected, the tests "DCBinaryOneCL1" and "DCNormalPL1CL1" were each executed at least once with the result "passed". The test "DCNormtoLowPLC1" was started but aborted before its automatic completion.

5.1.5 Activation/Deactivation Procedure

(§ A.6.2 - ETS300 012)

In order to achieve error-free transfer of data and information on the S_0 bus it is necessary to activate the physical layer (layer 1) according to a previously declared sequence and to build the higher layers onto it (layer 2: link layer, layer3: network layer). With these tests, the status of the layer 1 component is checked with all possible states.

The test object which is in the current state receives the stimulus signal and assumes the state specified under "Next state". All tests with their purposes (original text according to CTS2) are listed below.

The following tests are available:

Test No.	Ausgangs-zustand	Stimulus	Bemer-kung	Folge-zustand	INFO gesendet	CTS-2 Name Appendix B1	Zweck
1a	F1	Power	1/9	F2	INFO 0	ISDN1/AD/F1/AD1aF1_PS&LP-on	To check the reaction to the appearance of power on an IUT is state F1
1b	F1.0	Power	1/6/9	F1.1	INFO 0	ISDN1/AD/F1/AD1bF10_LP-on	To check the reaction to the appearance of local power on an IUT is state F1.0
1c	F1.1	Loss of power	6/9	F1.0	INFO 0	ISDN1/AD/F1/AD1cF11_LP-off	To check that IUT is inactive when there is a loss in state F1.1
1d	F1.1	Power	1/9	F2	INFO 0	ISDN1/AD/F1/AD1dF11_PS-on	To check the appearance of power S on IUT in state F1.1
2	F1.1	T3 expires	2/6	F1.1	INFO 0	ISDN1/AD/F1/AD2F11_CHK_T3	To check the expiration of T3 in state F1.1
3a	F2	Loss of power	9	F1 or F1.1	INFO 0	ISDN1/AD/F2/AD3aF2_PS-off	To check that IUT is brought to state F1 or F1.1 in case of disappearance of power S (no local power)
3b	F2	Loss of power	9	F1 or F1.0	INFO 0	ISDN1/AD/F2/AD3bF2_LP-off	To check that IUT is brought to state F1 or F1.0 in case of disappearance of local power
4	F2	RX INFO 0	4	F3	INFO 0	ISDN1/AD/F2/AD4F2_RX-IO	To check that IUT is brought to state F3 when receiving INFO 0 in state F2
5	F2	RX INFO 2		F6	INFO 3	ISDN1/AD/F2/AD5F2_RX-I2	To check that IUT is brought to state F6 when receiving INFO 2 in state F2
6	F2	RX INFO 4		F7	INFO 3	ISDN1/AD/F2/AD5F2_RX-I4	To check that IUT is brought to state F7 when receiving INFO 4
7	F2	RX any signal	3	F2	INFO 0	ISDN1/AD/F2/AD7F2_RX-IX	To check that IUT stays in state F2 when receiving INFO X in state F2
8	F2	T3 expires	6	F2	INFO 0	ISDN1/AD/F2/AD8F2_CHK_T3	To check the expiration of T3 in state F2
9a	F3	Loss of power	9	F1 or F1.1	INFO 0	ISDN1/AD/F3/AD9aF3_PS-off	To check that IUT is brought to state F1 or F1.1 in case of disappearance of power S
9b	F3	Loss of power	9	F1 or F1.0	INFO 0	ISDN1/AD/F3/AD9bF3_LP-off	To check that IUT is brought to state F1 or F1.0 in case of disappearance of local power
10	F3	PH-AR		F4	INFO 1	ISDN1/AD/F3/AD10F3_PH-AR	To check that IUT is brought to state F4 when receiving a PH-AR
11	F3	RX INFO 0	4	F3	INFO 0	ISDN1/AD/F3/AD11F3_RX-IO	To check that IUT stays in state F3 when receiving INFO 0
12	F3	RX INFO 2		F6	INFO 3	ISDN1/AD/F3/AD12F3_RX-I2	To check that IUT is brought to state F6 when receiving INFO2
13	F3	RX INFO 4		F7	INFO 3	ISDN1/AD/F3/AD13F3_RX-I4	To check that IUT is brought to state F7 when receiving INFO4
14	F3	RX any signal	3	F3	INFO 0	ISDN1/AD/F3/AD14F3_RX-IX	To check that IUT stays in state F3 when receiving INFOX
15	F3	T3 expires	2	F3	INFO 0	ISDN1/AD/F3/AD15F3_CHK_T3	To check the expiration of T3 in state F3
16a	F4	Loss of power	9	F1 or F1.1	INFO 0	ISDN1/AD/F4/AD16aF4_PS-off	To check that IUT is brought to state F1 or F1.1 in case of disappearance of power S

16b	F4	Loss of power	9	F1 or F1.0	INFO 0	ISDN1/AD/F4/AD16bF4_LP-off	To check that IUT is brought to state F1 or F1.0 in case of disappearance of local power
[illegible]	F4	RX INFO 0	4	F4	INFO 1	ISDN1/AD/F4/AD17F4_RX-I0	To check that IUT stays in state F4 when receiving INFO 0 during T3
18	F4	RX INFO 2	7	F6	INFO 3	ISDN1/AD/F4/AD18F4_RX-I2	To check that IUT is brought to state F6 when receiving INFO 2 in state F4
19	F4	RX INFO 4	7	F7	INFO 3	ISDN1/AD/F4/AD19F4_RX-I4	To check that IUT is activated when receiving INFO 4 in state F4
20	F4	Rx any signal	3	F5	INFO 0	ISDN1/AD/F4/AD20F4_RX-IX	To bring IUT into state F5
21	F4	T3 expires	2	F3	INFO 0	ISDN1/AD/F4/AD21F4_CHK_T3	To check T3 in state F4
22a	F5	Loss of power	9	F1 or F1.1	INFO 0	ISDN1/AD/F5/AD22aF5_PS-off	To check that IUT is brought to state F1 or F1.1 in case of disappearance of power S
22b	F5	Loss of power	9	F1 or F1.0	INFO 0	ISDN1/AD/F5/AD22bF5_LP-off	To check that IUT is brought to state F1 or F1.0 in case of disappearance of local power
23	F5	RX INFO 0	4	F5	INFO 0	ISDN1/AD/F5/AD23F5_RX-I0	To check that IUT stays in state F5 when receiving INFO 0
24	F5	RX INFO 2		F6	INFO 3	ISDN1/AD/F5/AD24F5_RX-I2	To check that IUT is brought to state F6 when receiving INFO 2 in state F5
25	F5	RX INFO 4		F7	INFO 3	ISDN1/AD/F5/AD25F5_RX-I4	To check that IUT is activated when receiving INFO 4 in state F5
26	F5	RX any signal	3	F5	INFO 0	ISDN1/AD/F5/AD26F5_RX-IX	To check that IUT stays in F5 after receiving INFO X during T3 and returns to state F3 after expiration of T3
27	F5	T3 expires	2	F3	INFO 0	ISDN1/AD/F5/AD27F5_CHK_T3	To check expiration of T3 in state F6
28a	F6	Loss of power	9	F1 or F1.1	INFO 0	ISDN1/AD/F6/AD28aF6_PS-off	To check that IUT is brought to state F1 or F1.1 in case of disappearance of power S
28b	F6	Loss of power	9	F1 or F1.0	INFO 0	ISDN1/AD/F6/AD28bF6_LP-off	To check that IUT is brought to state F1 or F1.0 in case of disappearance of local power
28c	F6	Loss of power	8/9	F6	INFO 3	ISDN1/AD/F6/AD28cF6_PS-off	To check that IUT stays in state F6 in case of disappearance of power S
29	F6	Lost framing		F8	INFO 0	ISDN1/AD/F6/AD29F6_Lostfr	To check that IUT is brought to state F8 in case of lost framing
30	F6	PH-AR		F6	INFO 3	ISDN1/AD/F6/AD30F6_PH-AR	To check that a PH-AR generates no action from IUT in state F6 but has really been sent
31	F6	RX INFO 0	4	F3	INFO 0	ISDN1/AD/F6/AD31F6_RX-I0	To check that IUT is brought to state F3 when receiving INFO 0 in state F6
32	F6	RX INFO 2		F6	INFO 3	ISDN1/AD/F6/AD32F6_RX-I2	To check that IUT stays in state F6 when receiving INFO 2

Test No.	Ausgangs-zustand	Stimulus	Bemer-kung	Folge-zustand	INFO gesendet	CTS-2 Name Appendix B1	Zweck
33	F6	RX INFO 4		F7	INFO 3	ISDN1/AD/F6/AD33F6_RX-I4	To check that IUT is activated when receiving INFO 4 in state F6
34	F6	T3 expires	2	F6	INFO 3	ISDN1/AD/F6/AD34F6_CHK_T3	To check the expiration of T3 in state F6
35a	F7	Loss of power	9	F1 or F1.1	INFO 0	ISDN1/AD/F7/AD35aF7_PS-off	To check that IUT is brought to state F1 or F1.1 in case of disappearance of power S
35b	F7	Loss of power	9	F1 or F1.0	INFO 0	ISDN1/AD/F7/AD35bF7_LP-off	To check that IUT is brought to state F1 or F1.0 in case of disappearance of local power
35c	F7	Loss of power	8/9	F7	INFO 4	ISDN1/AD/F7/AD35cF7_PS-off	To check that IUT stays in state F7 in case of disappearance of power S
36	F7	Lost framing		F8	INFO 0	ISDN1/AD/F7/AD36F7_Lostfr	To check that IUT goes to state F8 after receiving INFO X
37	F7	RX INFO 0	4/5	F3	INFO 0	ISDN1/AD/F7/AD37F7_RX-I0	To check that IUT is brought to state F3 when receiving INFO 0 in state F7
38	F7	RX INFO 2		F6	INFO 3	ISDN1/AD/F7/AD38F7_RX-I2	To check that IUT is brought to state F6 when receiving INFO 2 in state F7
39	F7	RX INFO 4		F7	INFO 4	ISDN1/AD/F7/AD39F7_RX-I4	To check that IUT stays in state F7 when receiving INFO 4
40a	F8	Loss of power	9	F1 or F1.1	INFO 0	ISDN1/AD/F8/AD40aF8_PS-off	To check that IUT is brought to state F1 or F1.1 in case of disappearance of power S
40b	F8	Loss of power	9	F1 or F1.0	INFO 3	ISDN1/AD/F8/AD40bF8_LP-off	To check that IUT is brought to state F1 or F1.0 in case of disappearance of local power
41	F8	PH-AR		F8	INFO 0	ISDN1/AD/F8/AD41F8_PH-AR	To check that a PH-AR generates no action from IUT in state F8 but has really been sent
42	F8	RX INFO 0	4/5	F3	INFO 0	ISDN1/AD/F8/AD42F8_RX-I0	To check that IUT is brought to state F3 when receiving INFO 0 in state F8
43	F8	RX INFO 2		F6	INFO 3	ISDN1/AD/F8/AD43F8_RX-I2	To check that IUT is brought to state F6 when receiving INFO 2 in state F8
44	F8	RX INFO 4		F7	INFO 3	ISDN1/AD/F8/AD44F8_RX-I4	To check that IUT is activated when receiving INFO 4 in state F8
45	F8	RX any signal	3	F8	INFO 0	ISDN1/AD/F8/AD45F8_RX-IX	To check that IUT stays in state F8 when receiving INFO X
46	F8	T3 expires	2	F3	INFO 0	ISDN1/AD/F8/AD46F8_CHK_T3	To check expiration of T3 in state F8

No.	Bemerkung / Note
1	Da der Prüfling IUT auf verschiedene Weisen gespeist werden kann, ist es sinnvoll, den Prüfling mit der durch ihn detektierbaren Speisung zu versorgen (PS1, PS2, local power)
2	T3 ist Implementations-abhängig und darf 30s nicht überschreiten.
3	"any signal" kann durch jedes Bitmuster erzeugt werden, auf das der Prüfling gem. §A.6.3.1.2-ETS 300_012 nicht synchronisieren kann.
4	Für die Testanwendung soll INFO 0 durch ein Sinus-Signal mit U_{SS}=100mV und 2kHz <f<1MHz simuliert werden. Das TE soll innerhalb von 250µs bis 25ms darauf reagieren. Bei Verwendung der Option Leitungsnachbildung 7KK1413-2AA kann die Störquelle im Menü gewählt und zugeschaltet werden.
5	Die korrepondierende PH-DI Meldung wird an Schicht 2 nach dem Empfang von INFO 0 nur dann gegeben, wenn die Schicht 1 nicht innerhalb von 500ms bis 1s wieder in den aktiven Zustand zurückkehrt.
6	Nur anwendbar für solche TE, die lokal gespeist sind bzw. PS1 oder PS2 detektieren können.
7	Wenn INFO 2 oder INFO 4 nicht innerhalb 5ms nach seinem Auftreten erkannt wird, muß das TE nach F5 wechseln. Das Ergebnis ist 5ms nach der Erzeugung des Stimulus zu überprüfen.
8	TE, die lokal gespeist werden oder PS1 bzw. PS2 detektieren können, dürfen nach dem Ereignis "Verlust der Speisespannung/disappearance of Power S" im Zustand F6 und F7 den Zustand nicht wechseln.
9	*Für die Tests, für die PS-OFF bzw. PS-ON gefordert wird, wird automatisch die Fernspeisung PS ab- bzw. eingeschaltet. Für die Tests, für die LP-OFF bzw. LP-ON gefordert wird wird an der Buchse TRIG OUT logisch "0" für OFF und "1" für ON ausgegeben (TTL, 25*

Bem.: Die Buchse TRIG OUT ist bei einigen Geräten irrtümlich mit TRIG IN bezeichnet.

The tests of the test group Activation/deactivation are selected as follows:

Measuring mode :

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Test mode :

ACTIVATION/DEACTIVATION

Activation of the test group via:

START/STOP

In the main window of the display, all required tests appear in dependency of the TEST SUITE PARAMETERS set previously. Due to limited space, the test numbers of the table above are used as short designations for the individual tests. If the TEST SUITE PARAMETER "PC-PS" is set on "yes", the following tests are available for selection:

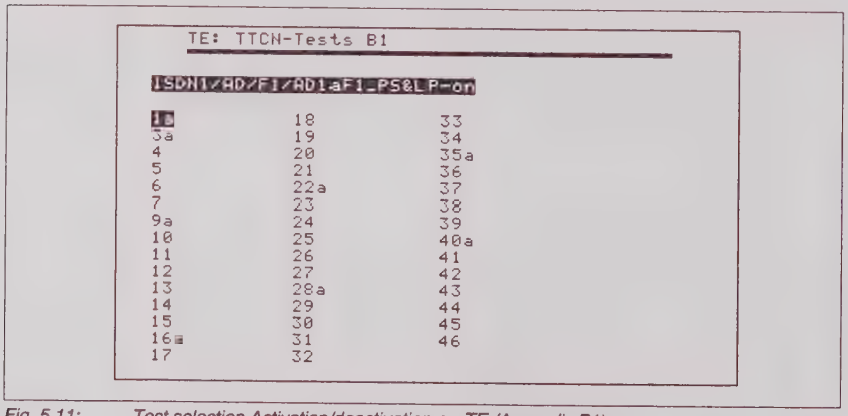


Fig. 5.11: Test selection Activation/deactivation on TE (Appendix B1)

The tests can now be selected for a sequence and started as described in Section 4.2.3. After running several tests, the following display is possible:

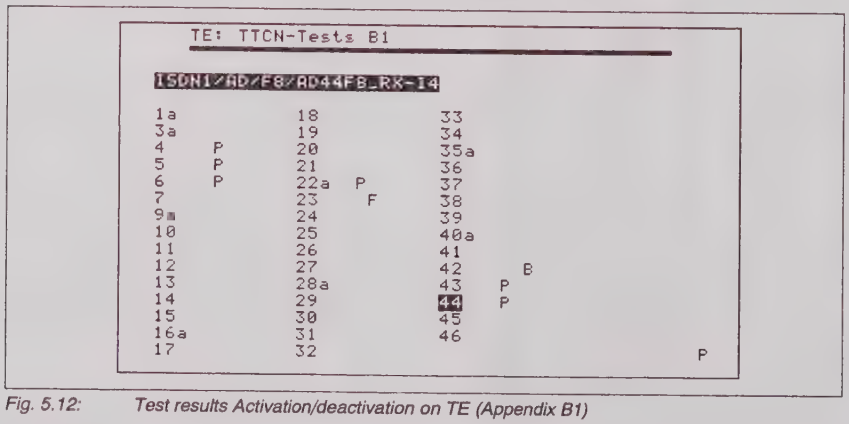


Fig. 5.12: Test results Activation/deactivation on TE (Appendix B1)

The currently selected test has the designation "ISDN1/AD/F8/AD44F8_RX-I4" and the test number 44. It was completed with the result "passed". The test numbers 4,

5, 6, 22a and 43 also "passed", while test number 23 "failed" and test number 42 was aborted before automatic completion of the sequence.

5.1.6 Timer Tests

(§ A.6.2 - ETS300 012)

Layer 1 establishment and clearance procedures should be terminated within a declared time. This prevents terminal equipment from remaining unnecessarily in an intermediate status during activation, deactivation and in the event of a Frame loss and thus blocking the system. These tests are also described completely in CTS and ETSI.

The following tests can be executed (the original CTS texts are used in the table):

Test No.	CTS-2 Name	Purpose / Zweck
1	ISDN1/TI/F3/TIF3info2	To check the value of the TE activation times in the waiting for signal state
1a	ISDN1/TI/F3/TIF3info2_inv	To check the value of the TE activation times in the waiting for signal state
2	ISDN1/TI/F3/TIF3info4	To check the value of the TE activation times in the waiting for signal state
3	ISDN1/TI/F4/TIF4info2	To check the value of the TE activation times in the waiting for signal state
4	ISDN1/TI/F4/TIF4info4	To check the value of the TE activation times in the waiting for signal state
5	ISDN1/TI/F4/TIF4infoX	To check the value of the TE activation times in the waiting for signal state
6	ISDN1/TI/F3/TItimerT3	To check the value of the timer T3
7	ISDN1/TI/F6/TIF6physdeact	To check the value of the TE deactivation times
8	ISDN1/TI/F7/TIF7physdeact	To check the value of the TE deactivation times
9	ISDN1/TI/F7/TIF7compdeact1	To check the value of the timer when leaving state F7 upon the reception of INFO 0
10	ISDN1/TI/F7/TIF7compdeact2	To check the value of the timer when leaving state F7 upon the reception of INFO 0
11	ISDN1/TI/F8/TIF8compdeact1	To check the value of the timer when leaving state F8 upon the reception of INFO 0
12	ISDN1/TI/F8/TIF8compdeact2	To check the value of the timer when leaving state F8 upon the reception of INFO 0

The tests of this test group are selected as follows:

Measuring mode :

TTCN-TESTS APPENDIX B1

Test mode :

TIMER TESTS

Activation of the test group via

START/STOP

All tests required in dependency of the TEST SUITE PARAMETER "PC-T309" set previously are displayed in the main window. If the timer 309 is implemented in the test object, the following display appears on the screen of the K1403:

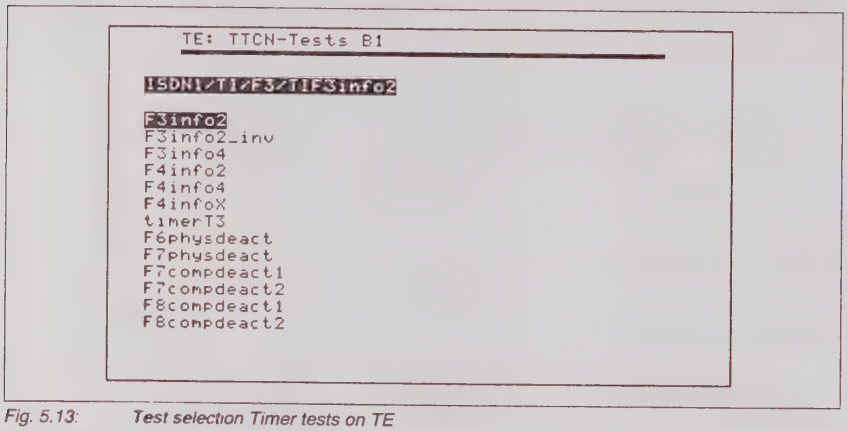


Fig. 5.13: Test selection Timer tests on TE

The tests can now be selected for a sequence and started as described in Section 5.1.3. After starting all tests, the following display is possible:

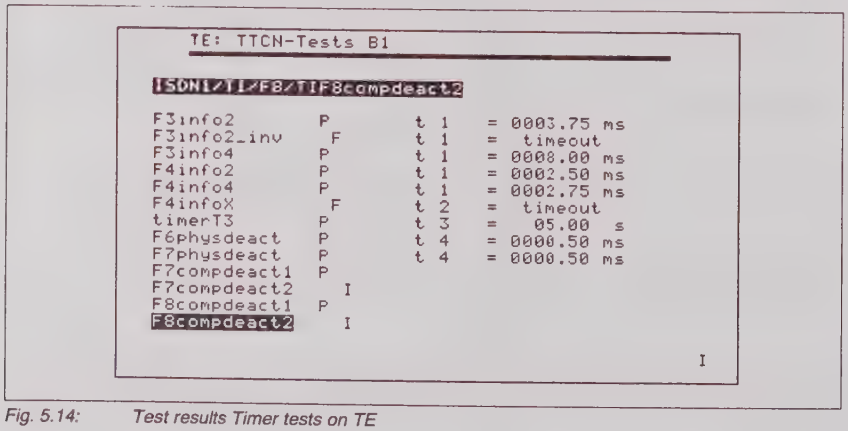

TE: TTCN-Tests B1
ISDN1/T1/F8/TIF8compdeact2
F3info2 P t 1 = 0003.75 ms
F3info2_inv F t 1 = timeout
F3info4 P t 1 = 0008.00 ms
F4info2 P t 1 = 0002.50 ms
F4info4 P t 1 = 0002.75 ms
F4infoX F t 2 = timeout
timerT3 P t 3 = 05.00 s
F6physdeact P t 4 = 0000.50 ms
F7physdeact P t 4 = 0000.50 ms
F7compdeact1 P
F7compdeact2 I
F8compdeact1 P
F8compdeact2 I
I

Fig. 5.14: Test results Timer tests on TE

The test last selected and executed was "F8compdeact2". It was completed with the result "inconclusive", as was the test "F7compdeact2". The tests "F3info2_inv" and

"F4infoX" received the result "failed". All other tests "passed".

Additionally, in this test group the corresponding activation or deactivation time obtained during the test is displayed to the right of the individual test results. The times t1 to t4 stand here for the timers defined in CTS-2, "TIMER_1"; "TIMER_2", "TIMER_3" or "TIMER_4". If the activation or deactivation time exceeds the defined timer value, the entry "timeout" appears next to the result "failed" instead of a time value.

5.1.7 Frame Alignment Tests

(§ A.6.3 - ETS300 012)

In order to retain the existing data and information transfer on the S_0 bus, an IUT which is already active should no longer transmit in the event of a Frame loss and should assume a declared status. This case may occur with brief interferences on the S_0 bus such as e.g. when inserting or removing a TE or in the event of a power fault. It is to resume the active status again as long as the declared normal conditions exist at its receiver input.

In this test, the module sends the good/bad frames declared by CTS-2 for Frame alignment/loss and logs the status of the test object depending on the received information.

The following tests can be carried out:

Test No.	CTS-2 Name	Purpose / Zweck
1	ISDN1/FA/F7/FAinfA_1fr	To test the no loss of frame alignment upon receipt of one bad frame
2	ISDN1/FA/F7/FAinfB_1fr	To test the no loss of frame alignment upon receipt of one bad frame
3	ISDN1/FA/F7/FAinfD_1fr	To test the no loss of frame alignment upon receipt of one bad frame
4	ISDN1/FA/F7/FAinfA_kfr	To test the number k of bad frames necessary for loss of frame alignment
5	ISDN1/FA/F7/FAinfB_kfr	To test the number k of bad frames necessary for loss of frame alignment
6	ISDN1/FA/F7/FAinfD_kfr	To test the number k of bad frames necessary for loss of frame alignment
7	ISDN1/FA/F7/FAregain	To test regain of frame alignment

The tests of this test group are selected as follows:

Measuring mode :

```
TTCN-TESTS APPENDIX B1
```

Test mode :

```
FRAME ALIGNMENT
```

Actiavtion of test group via

```
START/STOP
```

All required tests are displayed in the main window. The selection of the Frame alignment tests is independent of any TEST SUITE PARAMETER. Thus, the following display always appears on the screen of the K1403:

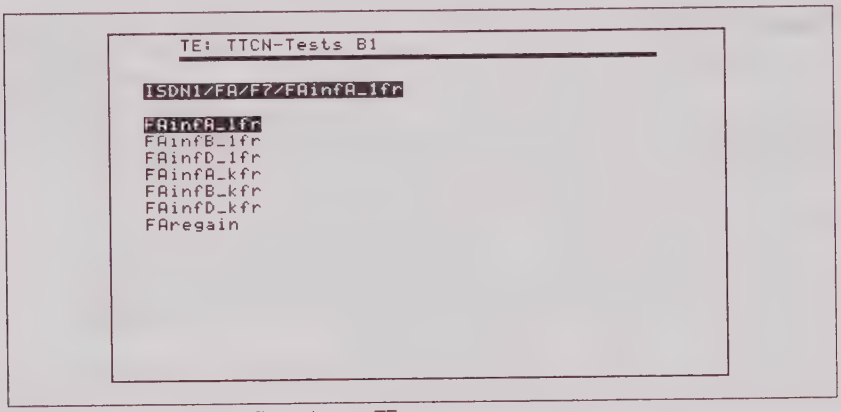


Fig. 5.15: Test selection Frame loss on TE

The results of the tests for Frame loss especially depend on the correct setting of the TEST SUITE PARAMETERS "PX_N" and _PX_M".

Parameters "PX_N" and "PX_M" must be set exactly in accordance with manufacturer's instructions for the test object (PICS/PIXIT). The two values each designate the number of frames which lead to loss or regaining of frame synchronization.

The tests can now be selected for a sequence and started. After starting all tests, the following results display is possible:

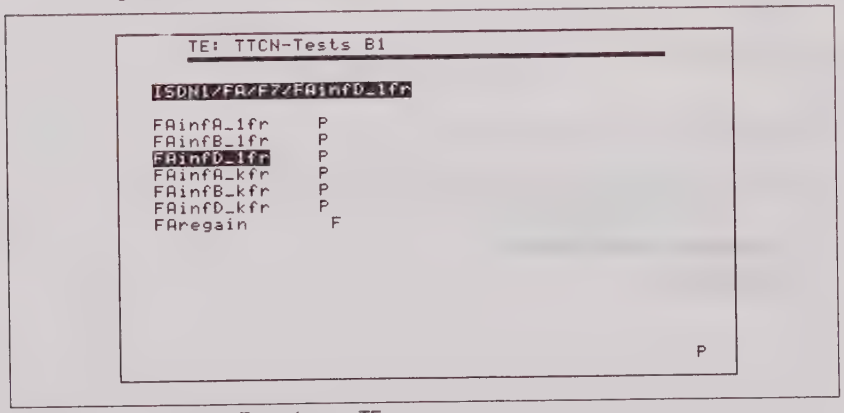


Fig. 5.16: Test results Frame loss on TE

The last test selected and executed is "FAinfD_1fr". It was completed with the result "passed". This result was also entered as auxiliary information in the lower right corner of the main window of the display. Except for "FAregain", which "failed", all tests were completed with a positive result.

5.1.8 Multi-Framing Procedures

(§ A.6.3.3 - ETS300 012)

To enable the transfer of data and information on the S_0 bus, a Multiframe bit sequence is defined with S and Q bits in addition to the B-channels and the D-channel. Information specific to the S_0 bus layer 1 is exchanged here such as e.g. selftest requests or the failure of the phantom supply. The Multiframe synchronization bit is the M bit sent by the NT which is set in every twentieth S_0 frame. The M bit is otherwise binary "1", i.e. has a zero level. The Multiframe bit of the TE is the FA bit which is transmitted as the Q bit with every fifth frame. Otherwise the FA bits received from the NT would be reflected in the remaining four frames. The transmission rate of the Q channel is 800 bit/s.

In the test on the TE, the Q bit is compared with the transmitted FA bit and logged. Only one test is defined according to CTS.

Test No.	CTS-2 Name	Purpose / Zweck
1	ISDN1/MU/F7/MUltiframe	To test the IUT correctly executes the frame alignment procedures

This test is selected as follows:

Measuring mode :

`TTCN-TESTS APPENDIX B1`

Test mode :

`MULTI-FRAMING`

Activation of test display:

`START/STOP`

The following display appears in the main window:

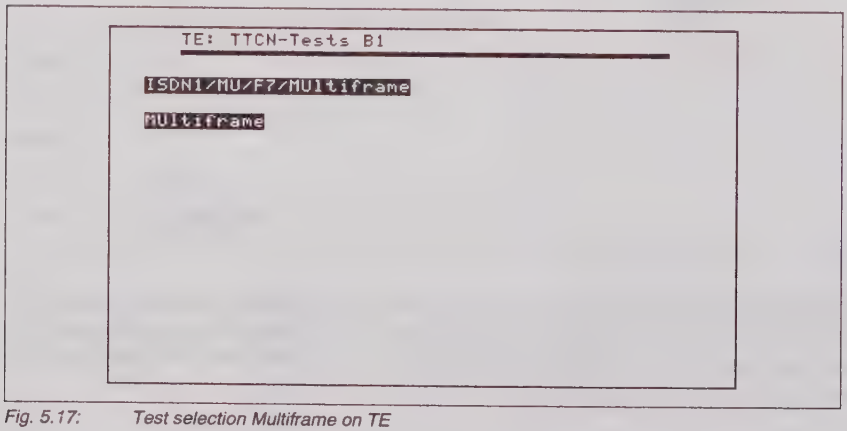


Fig. 5.17: Test selection Multiframe on TE

Since only one test is available, the process of test selection is omitted, and no cursors are displayed. If the test was started and completed with the result "passed", the following results display appears on the screen:

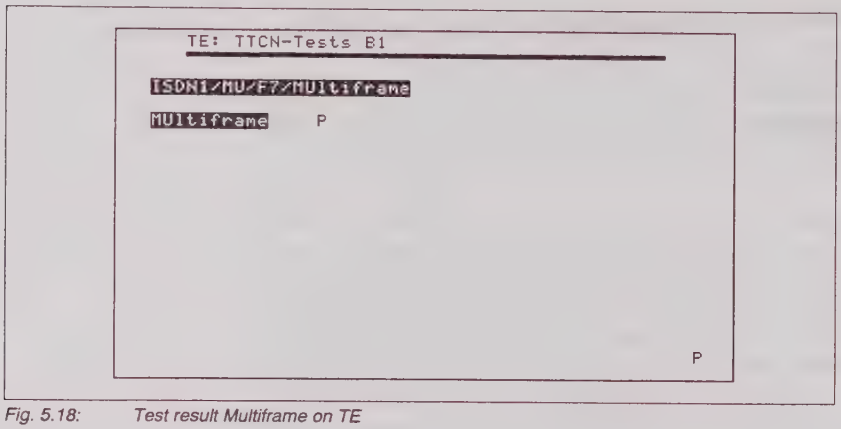


Fig. 5.18: Test result Multiframe on TE

B-channel content

(§ A.6.4 - ETS300 012)

Terminal equipment already activated in layer 1 must not transmit data (binary "1") in the B-channels until the channels have been enabled for use by the higher layers. For example, if an additional TE is inserted on an already active S_0 bus, it must not interfere with a connection which has already been established.

This B-channel monitoring test is only carried out on TEs. The test duration is 100 ms. Only one test is defined according to CTS.

Test No.	CTS-2 Name	Purpose / Zweck
1	ISDN1/BC/F7/BCBinaryOne	To check the B-channel contains the correct interframe time fill from the TE

This test is selected as follows:

Measuring mode :

`TTCN-TESTS APPENDIX B1`

Test mode :

`B-CHANNEL CONTENT`

Activation of test display

`START/STOP`

The following display appears in the main window of the screen:

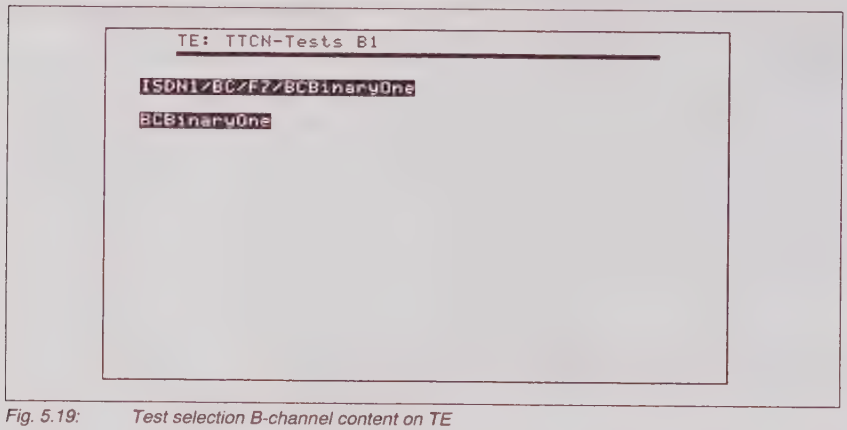


Fig. 5.19: Test selection B-channel content on TE

Since only one test is available, the process of test selection is omitted, and no cursors are displayed. If the test was started and completed with the result "passed", the following results display appears on the screen:

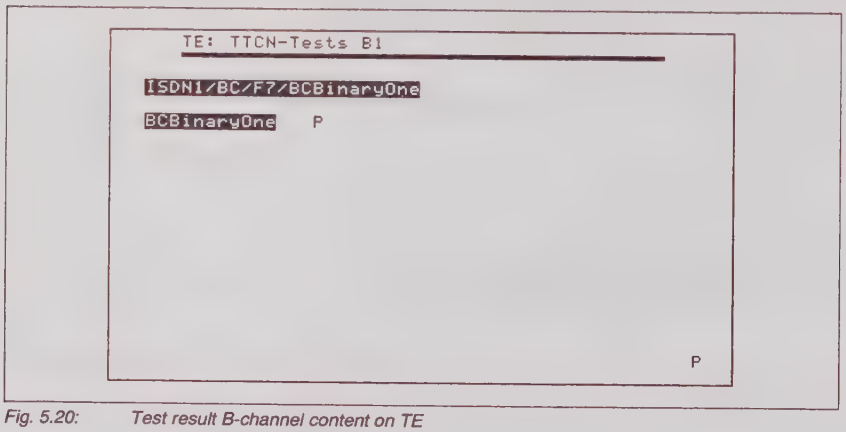


Fig. 5.20: Test result B-channel content on TE

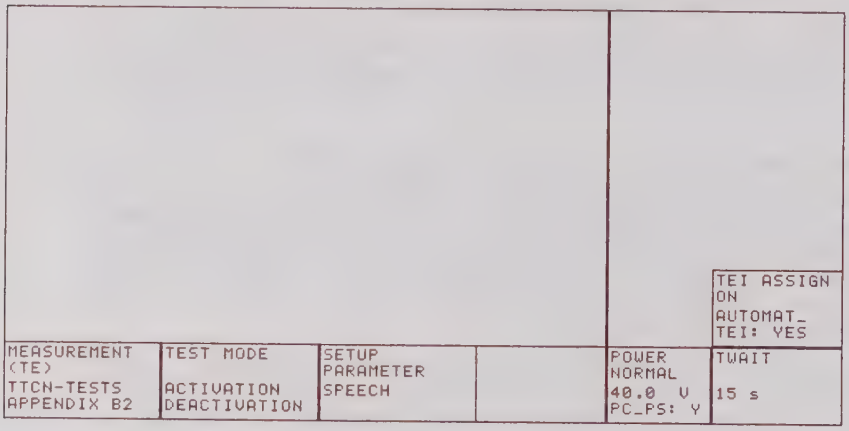
5.1.10 Tests Defined in TTCN (Appendix B2)

The tests described in Appendix B2 can only be executed with additional software. This software is available under the order no. 7KK1403-6AC10.

All tests for reactions of test objects which cannot be measured directly at the S_0 interface are defined in the Appendix B2 in TTCN of the CTS-2 document. This includes for example all reactions that an event in layer 1 (physical level) triggers in higher levels (software) of the test object. The triggers of these reactions are called PRIMITIVES. Thus you can, for instance, determine for "CHK_F7_PHAI", whether layer 1 of a TE in status F7 triggers a layer 2 Basic interconnection with "PH-AI-PRIMITIVE" after picking up the receiver.

Since the Appendix B2 tests are defined in the same way as the tests in Appendix B1 in TTCN, the test sequence with the K1403 is also nearly the same. In this section, only the differences between the tests in Appendix B1 are described.

The menu display is almost identical to the menu display from (Appendix B1). In the submenu TEST MODE, however, only two test groups are available.



Setting parameters (MENU)

MEASUREMENT (TE)
BASIC INTER-CONNECTION T.
BIN.ORG. OF FRAME
TTCN-TESTS APPENDIX B1
TTCN-TESTS APPENDIX B2

TEST MODE	INFORM. TRANS. CAPABILITY	TEST SUITE PARAMETER	TWAIT
D-CHANNEL ACCESS CONTR.	SPEECH	MENU	EDIT: 0...250s
ACTIVATION DEACTIVATION	AUDIO 3,1 kHz		
	DATA		
	AUDIO 7,0 kHz		
	VIDEO		

TEI ASSIGN	POWER
ON	NORMAL
OFF	RESTR:
EXTERNAL	EXTERNAL

Only with additional software

TTCN-TESTS APPENDIX B2

Dependencies

The following dependencies are present in this menu:

POWER FEEDING		
NORMAL	RESTRICTED	EXTERNAL
EDIT	EDIT	-
40V	40V	-

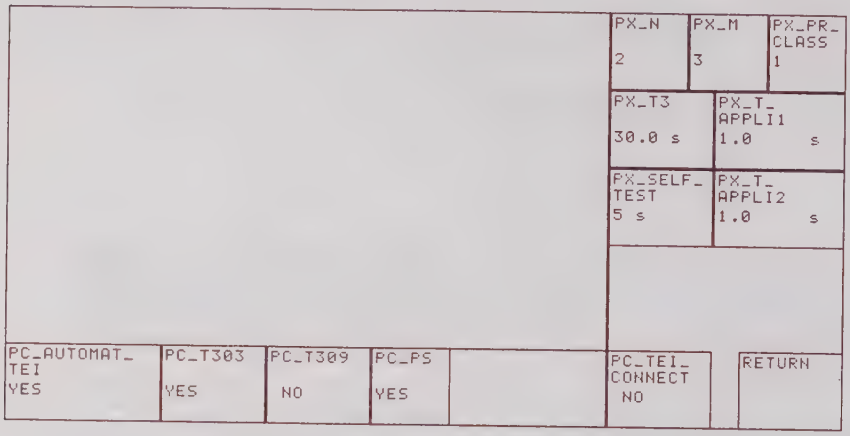
The MEASUREMENT PARAMETERS are integrated into the main menu of the functional tests just like the tests according to Appendix B1. They are identical with the parameters described in Appendix B1. The parameters INFORMATION TRANSMISSION CAPABILITY and TEI ASSIGNMENT are always important in the tests according to Appendix B2.

Submenu TEST SUITE PARAMETER of the SETUP MENU:

As for the tests according to Appendix B1, the menu **"TEST SUITE PARAMETER"** is called up via the key

`TEST SUITE PARAMETER`

The following display appears:



Setting parameters (MENU)

MEASUREMENT (TE)
BASIC INTER-CONNECTION
BIN. ORG. OF FRAME
TTCN-TESTS APPENDIX B1
TTCN-TESTS APPENDIX B2

TEST SUITE PARAMETER	PC_AUTOMAT_ TEI	PC_PS	PX_N	PX_M	PX_PR_ CLASS
MENU DISPLAY	YES	YES	EDIT: 2...250	EDIT: 3...250	1
	NO	NO			2

PC_ T303	PC_T3 09	PX_T3	PX_T_ APPLI1	PX_T_ APPLI2	PX_SELF_ TEST	PC_TEI_ CONNECT
YES	YES	EDIT: 1...30 s	EDIT: 0...600 s	EDIT: 0...600 s	EDIT: 0....4400 s	NO
NO	NO					YES

PC_DE	PX_T309
YES	EDIT
NO	

Only with additional software

TTCN-TESTS APPENDIX B2

Dependencies

PC_AUTOMAT_TEI	
YES	NO
PC_TEI_CONNECT	-
NO	-
YES	-

PC_PS	
YES	NO
-	PC_DE
-	YES
-	NO

PC_T309	
YES	NO
PX_T309	-
EDIT	-

Description of parameters

In this menu, four more TEST SUITE PARAMETERS are available than in the case of the tests according to Appendix B1. The meaning of these variables and their PICS/PIXIT numbers are listed in the table below.

Name	Type	PICS/ PIXIT	Comment
PC_T303	B	N6/3	TRUE if Timer T303 is implemented
PX_T_309	V	NX1/7	Duration of timer T309 if implemented
PX_T_APPLI1	V	PX2/7	Duration of application temporisation on B-channel if implemented, to establish a call
PX_T_APPLI2	V	PX2/8	Duration of application temporisation on B-channel if implemented, to disconnect a call

In the column **Type**, the letter **B** stands for a Boolean variable, and **V** for an adjustable value.

The parameter PX_T_309 is available in the menu only if the timer T309 is also implemented in the TE (PC_T309 = YES).

After setting the TEST SUITE PARAMETERS, return to the functional tests main menu using

RETURN

In order to start the functional tests defined in TTCN according to CTS-2 Appendix B2, one of the test groups described below must first be selected via

TEST MODE

To activate the selected **TEST GROUP** press

START/STOP

The TEST SUITE PARAMETERS set previously are evaluated and a selection of tests suitable for the test object connected is displayed in the main window of the K1403 display.

The individual tests of the selected test group can be started and controlled in the same way as the tests according to Appendix B1 using the **cursor softkeys** and the softkeys below.

START TEST

NEXT TEST

BREAK

Terminate the active status of the current test group by pressing

START/STOP

The test groups of the tests according to CTS-2 Appendix B2 are described below.

5.1.11 D-Channel Access Control

(§ A.6.1.3 to A.6.1.6 - ETS300 012)

The D-channel tests according to the CTS-2 definitions in Appendix B2 are exclusively ***D-echo channel procedures***. The purpose of the tests is to check whether a TE **no longer** transmits certain layer 2 or layer 3 frames after blocking the D-channel.

The following tests are available:

Test-no.	CTS-2 Name Appendix B2	Comment
1	ISDN1/CP/F7/CPF7DBLK_TEI	To check that IUT doesn't bufferize layer 2 frames ID_REQ when D-channel is blocked.
2	ISDN1/CP/F7/CPF7DBLK_SABME	To check that IUT doesn't bufferize layer 2 frames SABME when D-channel is blocked.
3	ISDN1/CP/F7/CPF7DBLK_SETUP	To check that IUT doesn't bufferize layer 3 frames SETUP when D-channel is blocked.
4	ISDN1/CP/F7/CPF7DBLK_DISC	To check that IUT doesn't bufferize layer 3 frames DISC when D-channel is blocked.

The tests of this test group are selected as follows:

Measuring mode (TE):

`TTCN-TESTS APPENDIX B2`

Test mode :

`D-CHANNEL ACCESS CONTROL`

Activation of test group via

`START/STOP`

All required tests in dependency of the **TEST SUITE PARAMETERS** "PX_PR_CLASS", "PC_AUTOMAT_TEI" and of the **measurement parameter** "TEI ASSIGNMENT" appear in the main window of the display. For "PX_PR_CLASS = 1", PC_AUTOMAT_TEI = YES" and "TEI ASSIGNMENT = YES" the following display appears on the screen of the K1403:

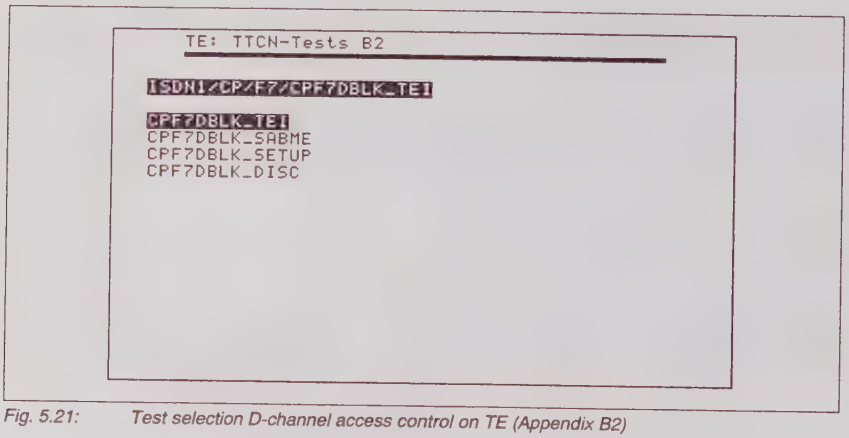


Fig. 5.21: Test selection D-channel access control on TE (Appendix B2)

The tests can now be selected for a test sequence and started according to Section 5.1.3 or 5.1.10. After several tests have been executed, the following results display is possible:

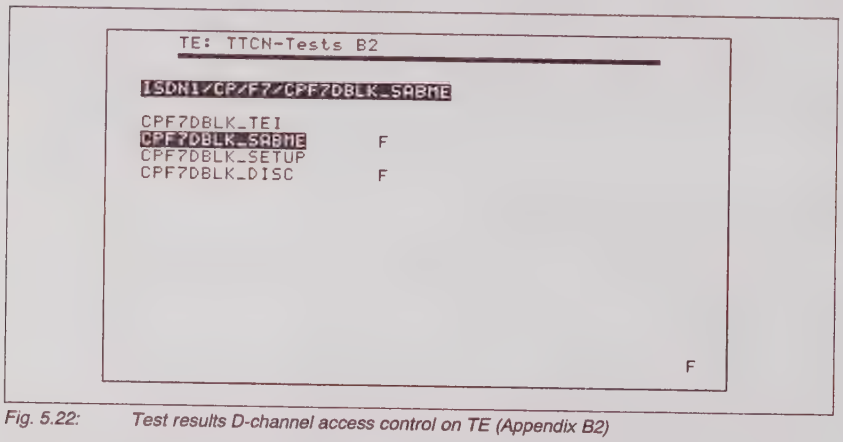


Fig. 5.22: Test results D-channel access control on TE (Appendix B2)

The test selected last is "CPF7DBLK_SABME". It ran at least once with the result (verdict) "failed". Before execution of this test, the test "CPF7DBLK_DISC" was also executed at least once with the result "failed".

5.1.12 Activation/Deactivation Procedure

(§ A.6.2 - ETS300 012)

In order to achieve error-free transfer of data and information on the S_0 bus it is necessary to activate the physical layer (layer 1) according to a previously declared sequence and to build the higher layers onto it (layer 2: link layer, layer 3: network layer). Using the tests according to CTS-2 Appendix B2, the reactions of the status machine of the layer 1 module to the various "PRIMITIVES" are checked for all possible states.

The table below lists all tests and their purpose (original text according to CTS-2).

The following tests are available:

Test No.	Ausgangs-zustand	Stimulus	Folge-zustand	INFO gesendet	CTS-2 Name Appendix B2	Zweck
4	F2	RX INFO 0	F3	INFO 0	ISDN1/CP/F2/CPF2MPHIICI0	To check that IUT is brought to state F3 when receiving Info 0 in state F2 and that it sends a MPH-II(c) primitive to ask for a TEI
5	F2	RX INFO 2	F6	INFO 3	ISDN1/CP/F2/CPF2MPHIICI2	To check that IUT is brought to state F6 when receiving Info 2 in state F2 and that it sends a MPH-II(c) primitive to ask for a TEI
6a	F2	RX INFO 4	F7	INFO 3	ISDN1/CP/F2/CPF2MPHIICI4	To check that IUT is brought to state F7 when receiving Info 4 in state F2 and that it sends a MPH-II(c) primitive to ask for a TEI
6b	F2	RX INFO 4	F7	INFO 3	ISDN1/CP/F2/CPF2PHAI	To check that IUT is brought to state F7 when receiving Info 4 in state F2 and that it sends a PH-AI primitive
9	F3	Loss of power	F1 or F1.0	INFO 0	ISDN1/CP/F3/CPF3MPHIID	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPH-II(d) primitive
10	F3	PH-AR	F4	INFO 1	ISDN1/CP/F4/CPF4Tlayer2	To check that IUT doesn't set on a layer 2 timer in the same time as T3
13	F3	RX INFO 0	F3	INFO 0	ISDN1/CP/F3/CPF3PHAI	To check that IUT is brought to state F7 when receiving Info 4 in state F4 and that a PH-AI primitive is sent
16	F4	Loss of power	F1 or F1.1	INFO 0	ISDN1/CP/F4/CPF4MPHIID	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPH-II(d) primitive
19	F4	RX INFO 4	F7	INFO 3	ISDN1/CP/F4/CPF4PHAI	To check that IUT is brought to state F7 when receiving Info 4 in state F4 and that a PH-AI primitive is sent
21	F4	T3 expires	F3	INFO 0	ISDN1/CP/F4/CPF4PHDI_T3exp	To check that IUT sends a PH-DI on T3 expiration
22	F5	Loss of power	F1 or F1.1	INFO 0	ISDN1/CP/F5/CPF5MPHIID	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPH-II(d) primitive
23	F5	RX INFO 0	F5	INFO 0	ISDN1/CP/F5/CPF5PHDI_I0T3	To check that IUT has no action on receipt of Info 0 in state F5
25	F5	RX INFO 4	F7	INFO 3	ISDN1/CP/F5/CPF5PHAI	To check that IUT is brought to state F7 when receiving Info 4 in state F4 and that a PH-AI primitive is sent
27a	F5	T3 expires	F3	INFO 0	ISDN1/CP/F5/CPF5PHDI_T3expa	To check that IUT sends a PHDI on T3 expiration
27b	F5	T3 expires	F3	INFO 0	ISDN1/CP/F5/CPF5PHDI_T3expb	To check that IUT sends a PHDI on T3 expiration
30a	F6	PH-AR	F6	INFO 3	ISDN1/CP/F6/CPF6PHARa	To check that a PHAR generates no action from IUT in state F6 but has really been sent
30b	F6	PH-AR	F6	INFO 3	ISDN1/CP/F6/CPF6PHARb	To check that a PHAR generates no action from IUT in state F6 but has really been sent

Test No.	Ausgangs-zustand	Stimulus	Folge-zustand	INFO gesendet	CTS-2 Name Appendix B2	Zweck
31a	F6	RX INFO 0	F3	INFO 0	ISDN1/CP/F6/CPF6PHDI_I0T3	To check that IUT goes from F6 to F3 on receipt of I0 while T3 is set on
31b	F6	RX INFO 0	F3	INFO 0	ISDN1/CP/F6/CPF6PHDI_I0	To check that IUT does send a PH-DI primitive upon receipt of Info 0 in state F6
33a	F6	RX INFO 4	F7	INFO 3	ISDN1/CP/F6/CPF6PHAIa	To check that IUT is brought to state F7 when receiving Info 4 in state F6 and that a PH-AI primitive is sent
33b	F6	RX INFO 4	F7	INFO 3	ISDN1/CP/F6/CPF6PHAIb	To check that IUT is brought to state F7 when receiving Info 4 in state F6 during T3 and that a PH-AI primitive is sent
34	F6	T3 expires	F6	INFO 3	ISDN1/CP/F6/CPF6PHDI_T3exp	To check that IUT sends a PH-DI on T3 expiration
36a	F7	Lost framing	F8	INFO 0	ISDN1/CP/F7/CPF7MPHEI_IX	To check MPH-EI primitives on receipt of Info X and then Info 4
36b	F7	Lost framing	F8	INFO 0	ISDN1/CP/F7/CPF7MPHEI_IXI2	To check MPH-EI primitives on receipt of Info X and then Info 2
36c	F7	Lost framing	F8	INFO 0	ISDN1/CP/F7/CPF7MPHEI_IXI0	To check MPH-EI and PH-DI primitives on receipt of Info X and then Info 0
36d	F7	Lost framing	F8	INFO 0	ISDN1/CP/F7/CPF7MPHEI_IXI2I0	To check MPH-EI and PH-DI primitives on receipt of Info X and then Info 2 and Info 0
36e	F7	Lost framing	F8	INFO 0	ISDN1/CP/F7/CPF7BUFa_IX	To watch consequenses of a layer 1 disturbance on layer 2 when IUT doesn't use T309
36f	F7	Lost framing	F8	INFO 0	ISDN1/CP/F7/CPF7BUFb_IX	To watch consequenses of a layer 1 disturbance on layer 2 when IUT uses T309
37	F7	RX INFO 0	F3	INFO 0	ISDN1/CP/F7/CPF7PHDI_I0	To check that IUT does send a PH-DI primitive upon receipt of Info 0 in state F7
38a	F7	RX INFO 2	F6	INFO 3	ISDN1/CP/F7/CPF7MPHEI_I2	To check MPH-EI primitives on receipt of Info 2 and then Info 4
38b	F7	RX INFO 2	F6	INFO 3	ISDN1/CP/F7/CPF7MPHEI_I2IX	To check MPH-EI primitives on receipt of Info 2 and then Info X
38c	F7	RX INFO 2	F6	INFO 3	ISDN1/CP/F7/CPF7MPHEI_I2I0	To check MPH-EI and PH-DI primitives on receipt of Info 2 and then Info 0
38d	F7	RX INFO 2	F6	INFO 3	ISDN1/CP/F7/CPF7MPHEI_I2IXI0	To check MPH-EI and PH-DI primitives on receipt of Info 2 and then Info X and Info 0
38e	F7	RX INFO 2	F6	INFO 3	ISDN1/CP/F7/CPF7BUFa_I2	To watch consequenses of a layer 1 disturbance on layer 2 when IUT doesn't use T309
38f	F7	RX INFO 2	F6	INFO 3	ISDN1/CP/F7/CPF7BUFb_I2	To watch consequenses of a layer 1 disturbance on layer 2 when IUT uses T309

Test No.	Ausgangs-zustand	Stimulus	Folge-zustand	INFO gesendet	CTS-2 Name Appendix B2	Zweck
40a	F8	Loss of power	F1 or F1.1	INFO 0	ISDN1/CP/F8/CPF8MPHIIDa	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPHII(d) primitive
40b	F8	Loss of power	F1 or F1.0	INFO 0	ISDN1/CP/F8/CPF8MPHIIDb	To check that IUT is brought to state F1.1 in case of disapearance of power S and that it sends a MPHII(d) primitive
41a	F8	PH-AR	F8	INFO 0	ISDN1/CP/F8/CPF8PHARa	To check that a PH-AR generates no action from IUT in state F8 but has really been sent
41b	F8	PH-AR	F8	INFO 0	ISDN1/CP/F8/CPF8PHARb	To check that a PH-AR generates no action from IUT in state F8 but has really been sent
42a	F8	RX INFO 0	F3	INFO 0	ISDN1/CP/F8/CPF8PHDI_I0T3	To check that IUT goes from F8 to F3 on receipt of I0 while T3 is set on
42b	F8	RX INFO 0	F3	INFO 0	ISDN1/CP/F8/CPF8PHDI_I0b	To check that IUT does send a PH-DI primitive upon receipt of Info 0 in state F8
44b	F8	RX INFO 4	F7	INFO 3	ISDN1/CP/F8/CPF8PHAIb	To check that IUT is brought to state F7 when receiving Info 4 in state F8 and that a PH-AI primitive is sent
44c	F8	RX INFO 4	F7	INFO 3	ISDN1/CP/F8/CPF8PHAIc	To check that IUT is brought to state F7 when receiving Info 4 in state F8 during T3 and that a PH-AI primitive is sent
46	F8	T3 expires	F3	INFO 0	ISDN1/CP/F8/CPF8PHDI_T3exp	To check that IUT returns to state F3 on T3 expiration

The tests of the test group Activation/deactivation are selected as follows:

Measuring mode :

TTCN-TESTS APPENDIX B2

Test mode :

ACTIVATION/DEACTIVATION

Activation of the test group via:

START/STOP

All required tests in dependency of the **TEST SUITE PARAMETERS** previously set appear in the main window of the display. Due to limited space, the test numbers from the table above were used as short designation for the individual tests. With the settings "PC_PS = YES", "PC_T309 = NO", "PC_AUTOMAT_TEI = YES", and the **measurement parameter** "TEI_ASSIGNMENT" set to "YES" the following tests are available:

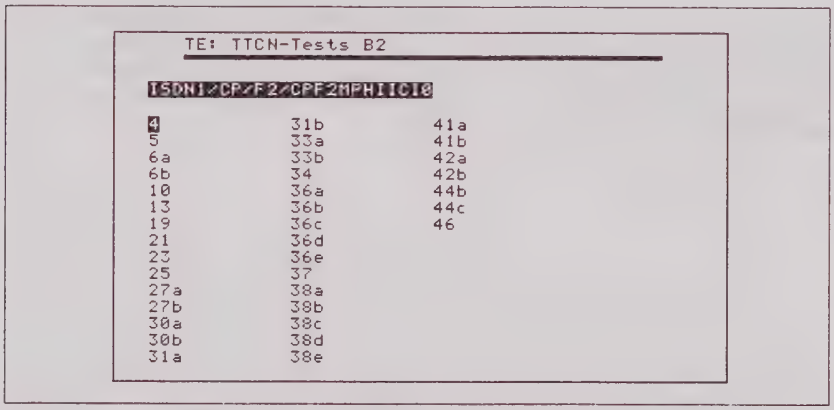


Fig. 5.23: Test selection Activation/deactivation on TE (Appendix B2)

The tests can now be selected for a test sequence and started. After running several tests, the following results display is possible:

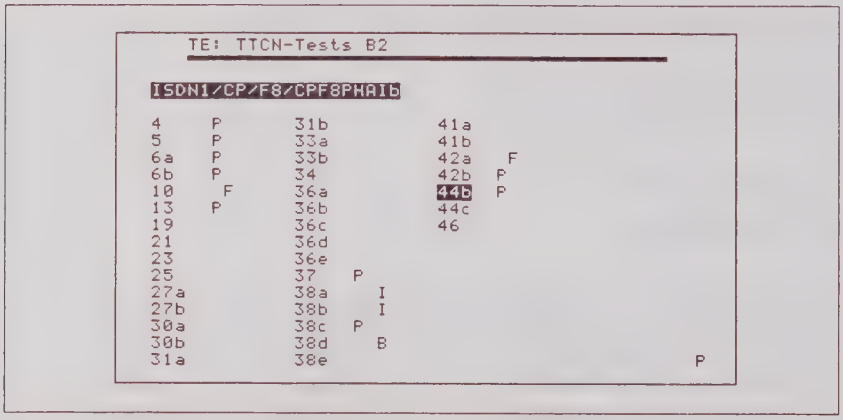


Fig. 5.24: Test results Activation/deactivation on TE (Appendix B2)

The test currently selected is designated "ISDN1/CP/F8PHAIb" with the test number 44b. It was completed with the result "passed". The same result was obtained for the tests with the numbers 4, 5, 6a, 6b, 13, 37, 38c and 42b. Tests 10 and 42a "failed", test number 38d was aborted before the automatic sequence was completed, and tests 38a and 38b received the result "inconclusive".

5.1.13 Receiver Sensitivity

(A.8.6.2.-ETS300 012)

There are four different bus configurations according to the CCITT recommendations. The connection of the Artificial Line Option 7KK1403-2AA (add-on board for K1403) means that the signal is delayed (delay time) and distorted (skin effect) in addition to being attenuated. Furthermore, the transmitted amplitude can be adjusted between -8 dB and +3 dB in increments of 0.1 dB. The terminal equipment to be tested should also function correctly with this inferior input signal and must not generate any bit errors (during a specific measuring period).

A PRBS signal is transmitted during the test, and the bit error count BEC and the bit error rate BER are measured on the test object with a loop switched on.

Since this measuring mode is assigned according to CTS and ETS to part of the measurement of the electrical properties of a TE, it can also be selected via the menu ELECTRICAL CHARACTERISTICS ON THE TE.

Menu: Measuring mode Receiver sensitivity

				DATA INTERNAL	PRBS 2^9 - 1
				MODE TIMELIMIT	TIME 60 s
MEASUREMENT (TE) RECEIVER SENSITIVITY	CLOCK INTERNAL	TRANSMITTER AMPLITUDE 0.0 dB	CHANNEL B1+ B2	POWER FEEDING NORMAL 42.0 V	WIRING CONFIG. CONFIG.4 (IDEAL)

Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
RECEIVER INPUT DELAY CHARAC.
CLOCK ACCURACY
TRANSM. OUTP. IMP. ACTIVE
PULSE UNBALANCE
OUTPUT PEAK CURRENT
JITTER
RECEIVER SENSITIVITY

CLOCK	TRANS-MITTER AMPLITUDE	CHANNEL	POWER FEEDING	DATA
INTERNAL	EDIT	B1	PASSIVE	INTERNAL
EXT: 5Hz 0.5UIpp	-1.5dB	B2	NORMAL	EXTERNAL
EXT: 20Hz 0.125UIpp	0dB	B1+B2	RESTR.	
EXT: 50Hz 0.05UIpp	+1.5dB		EXTERNAL	
EXT: 2kHz 0.05UIpp				
EXTERNAL 12.288MHz				

PRBS	MODE	TIME	WIRING CONFIG.
2^9-1	TIMELIMIT	EDIT	FREE CONFIG.
2^{11}-1	NO TIMELIMIT	60s	CONFIG. 1
2^{15}-1			CONFIG. 2
2^{20}-1			CONFIG. 3a
			CONFIG. 3b
			CONFIG. 4 (IDEAL)

The shaded softkeys CLOCK is disabled as long as no **Jitter** option is set.

JITTER OPTION

The WIRING CONFIGURATION is realized via the **Artificial Line Option**.

OPTION ARTIFICIAL LINE

Dependencies

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24V	24V	-
-	32V	32V	-
-	42V	42V	-

The feeding voltage can be edited in normal and emergency modes or set to the defined fixed values.

DATA	
INTERNAL	EXTERNAL
PRBS	---
2^9-1	---
2^{11}-1	---
2^{15}-1	---
2^{20}-1	---

One of the four different pseudo-random sequences PRBS can be selected if the internal source is selected for the data to be transmitted. The PRBS parameter thus depends on the selection of the DATA INTERNAL/EXTERNAL parameter. If DATA EXTERNAL is selected, an external source can be connected to sockets BU2 to BU4 on the front panel. It is not possible to determine the number of bit errors and the bit error rate in this case. The values therefore remain at zero during measurement and the conformance result is set to INCONCLUSIVE.

MODE	
TIMELIMIT	NO TIMELIMIT
TIME	---
EDIT	---
60s	---

The MODE parameter can be used to select a measurement with an adjustable duration (EDIT or 60 s) or a continuous measurement. If a measuring time is selected, the results are only determined for this interval and regenerated at the end of the interval. The bit error counter starts again at zero, and the error rate is only accumulated for the selected time.

To start measurement press

`START/STOP`

The following error or status messages may occur during the measurement:

Message	Comment
FKT : no INFO0 det.	No INFO0 has been received
FKT : no INFO1 det.	No INFO1 has been received
FKT : no INFO3 det.	No INFO3 has been received
FKT : INFO0 det.	INFO0 has been received
FKT : undef. INFO !	No defined INFO has been received
FKT : permanent ZERO	Binary "0" in the data channels
FKT : AIS	Binary "1" in the data channels
FKT : BITSLIP	Bit change in the data
FKT : LAYER 1 ERROR	Layer 1 error
FKT : wrong Amplitude	Receiver amplitude too large or too small
MEASUREM. aborted	Measurement aborted

If layer 1 cannot be activated on the test object or remains activated, the following messages are displayed alternatively:

`FKT : LAYER 1 ERROR`

`MEASUREM. aborted`

To start another measurement, e.g. following elimination of an error on the test object, the following key must be pressed twice:

`START/STOP`

Presentation of results

The results are displayed in the following form:

BE :	Count		Count of bit error counter; max 2^{32}
TIME:	Count	s	Count of expired seconds; max 2^{32}
BER:	Bit error rate	BE/s	Continuously calculated bit error rate; is deleted at the end of the set gate time and then regenerated.
Conformance	TRUE/FALSE/INC.		Is set to TRUE following the first expired, error-free gate time
Int. :	Count		Total of measured gate time (interval)
err. Int.:	Count		Total of measured gate times with bit errors

5.2 Functional Tests NT

The present hardware is already equipped for the functional tests on NT. The software includes the tests described in this chapter. The tests listed below according to ETSI 300_012 are not implemented, since no suitable test definitions exist for them (e.g. TTCN).

D-Echo channel response control procedure on NT

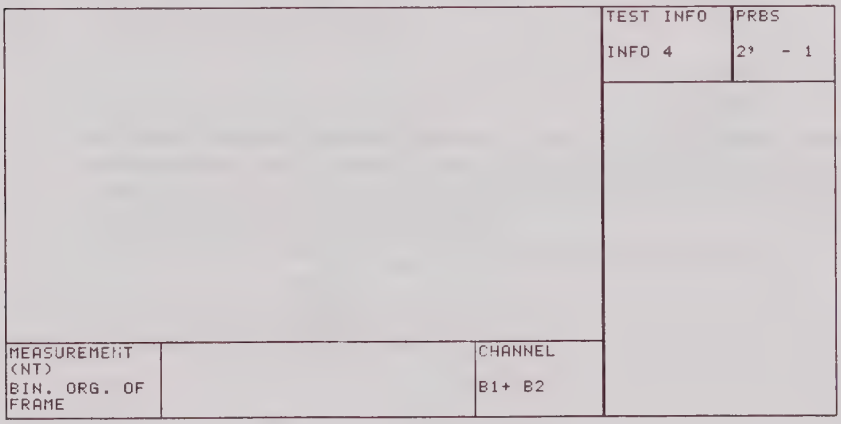
Activation/deactivation procedure on NT

Timer tests on NT

Frame alignment procedures on NT

Multiframing procedures on NT

5.2.1 Binary Organization of Frame



Setting parameters (MENU)

MEASUREMENT (NT)
BIN. ORG. OF FRAME

CHANNEL	TEST INFO	PRBS
B1	INFO 4	2^9 -1
B2	INFO 2	2^{11} -1
B1 + B2		2^{15} -1
B1 + B2 + D		2^{20} -1

Test A (A.5.4.2.2,ETS300 012)

Test B (A.5.4.2.2-ETS300 012)

Using this test, the frame structure setup of the INFO2 or INFO4 signal is tested. The signals on the S_0 bus are transmitted with the DC-free AMI Code. The signal consists of 3 levels (+Unorm, 0, -Unorm) is to fulfill certain criteria in a 48 bit S0-frame These criteria include the creation of the double code violation as well as the ternary level setting in the B-channels which is stimulated in the B-channel by sending a PRBS signal. The transmitted S_0 frame bits with their AMI level are displayed in the "envelope mode".

In order to check the B-channels, a data loop must be switched in the test object. To start measurement press

START/STOP

If no valid info is recognized, the S_0 data are not displayed in the envelope mode, but as single shots. Thus the S_0 data on the receiving end are visible to the user (oscilloscope function).

The conformance test is executed with the following parameter settings:

a)

Test INFO : INFO 4
Channel : B1 + B2 + D
PRBS : $2^9 - 1$
Result : Graphic

b)

Test INFO : INFO 2
Result : Graphic

The results display for various INFO2 or INFO4 frames are shown below. The asterisk for each bit position indicates that not all possible levels were recognized (envelope mode). The meaning of the 48 bits of a frame is indicated in the legend.

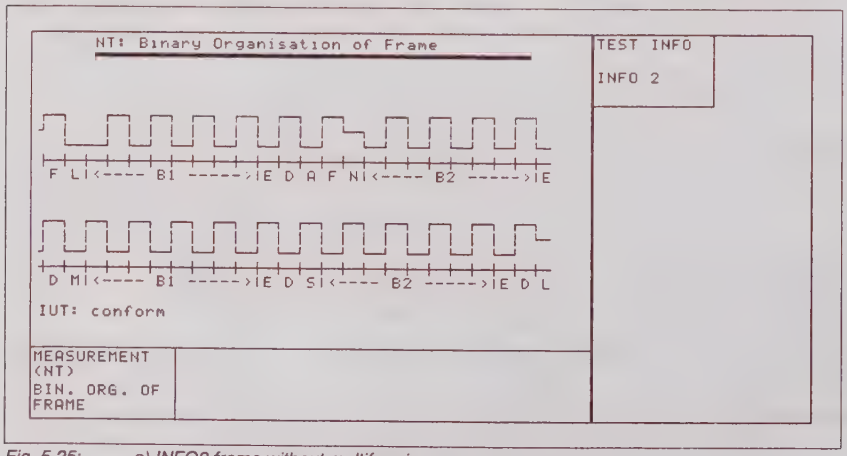


Fig. 5.25: *a) INFO2 frame without multiframing; result conforms, since all possible levels were recognized.*

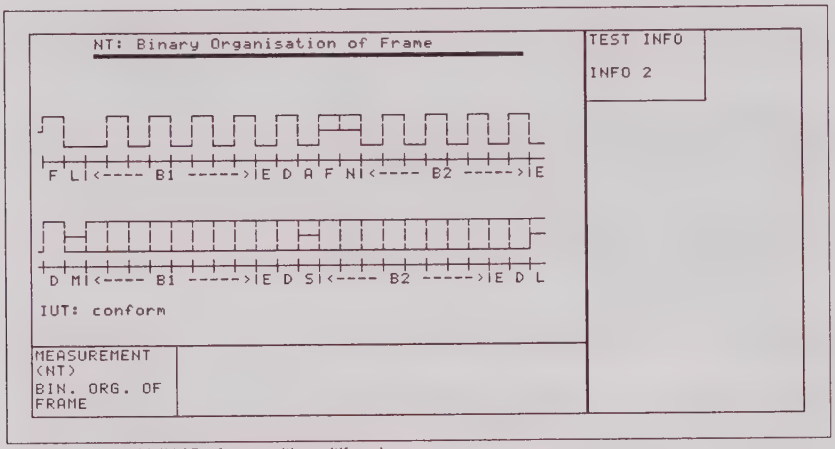


Fig. 5.26: *b) INFO2 frame with multiframing;*
result conforms since all possible levels were recognized.

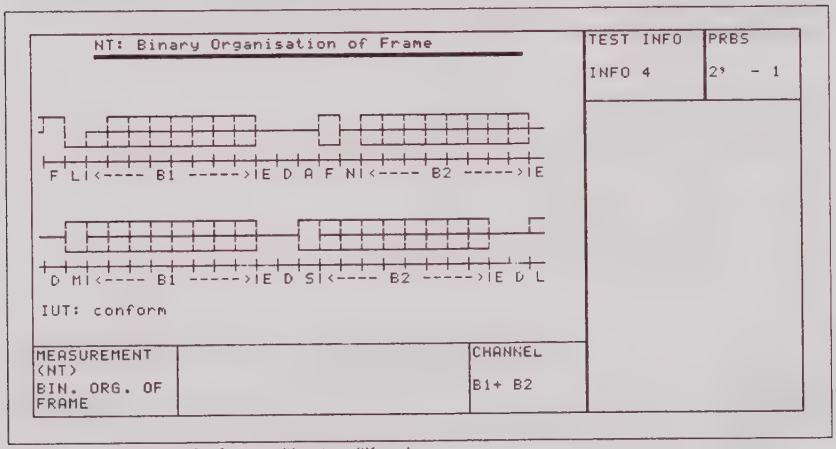


Fig. 5.27: a) *INFO4 frame without multiframing*

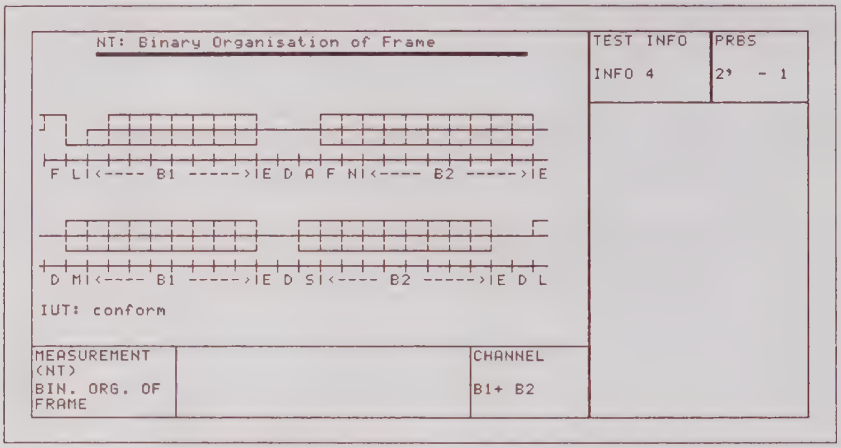


Fig. 5.28: b) *INFO4 frame with multiframing*

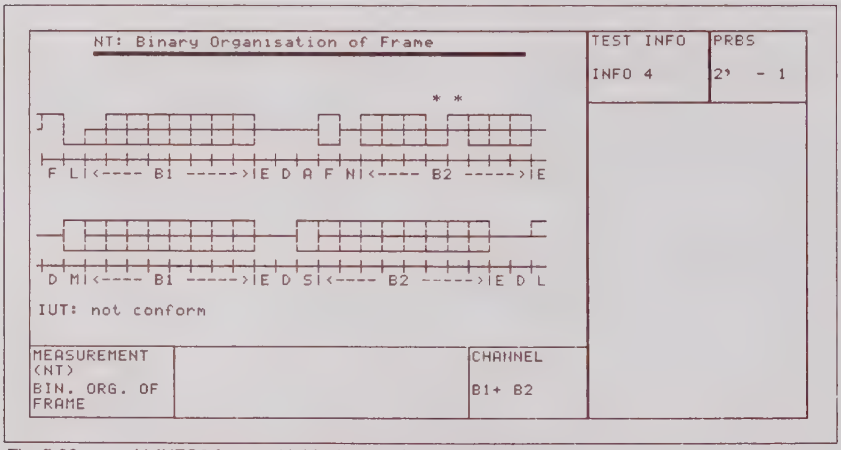


Fig. 5.29: *b) INFO3 frame with bit changes in the B-channels; conformance test for B1+B2; Result does not conform since not all possible levels were detected.*

5.2.2 Receiver Sensitivity

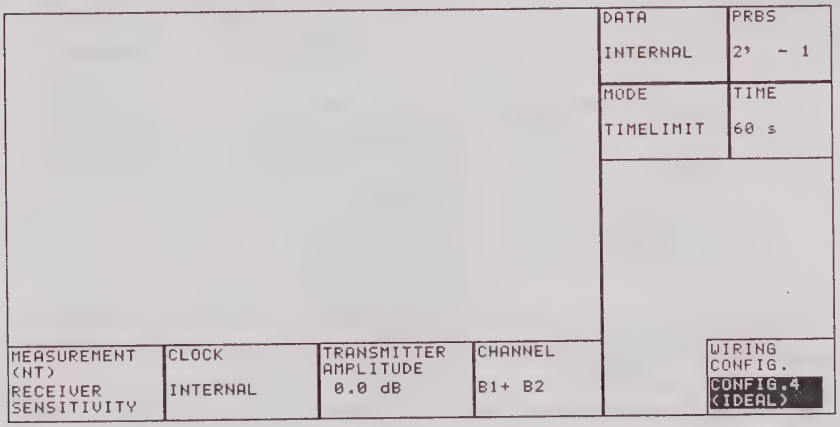
(A.8.6.2.-ETS300 012)

According to the CCITT recommendations, there are four different bus configurations. If the Artificial Line Option 7KK1403-2AA (add-on-board for K1403) is connected, the signal is not only attenuated but also delayed (delay time) and distorted (skin effect). Additionally, the transmitted amplitude can be adjusted from -8 dB to +3 dB in increments of 0.1 dB. The network terminator NT to be tested should also function properly with this inferior input signal and must not generate any bit errors (within a certain measuring time).

During the test a PRBS signal is transmitted and the bit error count BEC and the bit error rate BER are measured at the test object in the case of a switched-on loop or at the LT simulation to be used.

Since this measuring mode according to ETS is assigned to the measurements of electrical characteristics of an NT, it is selected via the menu ELECTRICAL CHARACTERISTICS ON NT.

Measuring mode Receiver sensitivity



Setting parameters (MENU)

MEASUREMENT (NT)
IMPEDANCE
UNBALANCE
PULSE SHAPE
TRANSM. OUTP. IMP. ACTIVE
OUTPUT PEAK CURRENT
JITTER
RECEIVER SENSITIVITY
RECEIVER INP. DELAY CHAR.

CLOCK	TRANS-MITTER AMPLITUDE	CHANNEL	DATA	PRBS
INTERNAL	EDIT	B1	INTERNAL	2^9-1
EXT: 5Hz 0.5UIpp	-1.5dB	B2	EXTERNAL	2^{11}-1
EXT: 2kHz 0.05UIpp	0dB	B1+B2		2^{15}-1
	+1.5dB			2^{20}-1

MODE	TIME	WIRING CONFIG.
TIMELIMIT	EDIT	FREE CONFIG.
NO TIMELIMIT	60s	CONFIG. 1
		CONFIG. 2
		CONFIG. 3a
		CONFIG. 3b
		CONFIG. 4 (IDEAL)

The shaded softkeys CLOCK is disabled as long as no **jitter** option is set.

JITTER OPTION

The WIRING CONFIGURATION is realized via the **Artificial Line Option**.

OPTION ARTIFICIAL LINE

Dependencies

DATA	
INTERNAL	EXTERNAL
PRBS	---
2^9-1	---
2^{11}-1	---
2^{15}-1	---
2^{20}-1	---

If you select the internal source for the data to be transmitted, one of four different pseudo-random sequences can be selected. The parameter PRBS is thus dependent on the selection of the parameter DATA INTERNAL/EXTERNAL. If you select DATA EXTERNAL, an external source can be coupled to the sockets BU2 to BU4 in the front panel of the unit. A statement about the number of bit errors and the bit error rate is not possible in this case. Therefore, the values remain on 0 during the measurement and the conformance result is set to INCONCLUSIVE.

MODE	
TIMELIMIT	NO TIMELIMIT
TIME	---
EDIT	---
60s	---

Via the parameter MODE, you can select between a measurement with a specific time setting (EDIT or 60s) or a continuous measurement. If you select a measuring time, the measured results are obtained only for this interval after which they are regenerated. The bit error count resumes at 0 and the error rate is accumulated only for the duration selected.

To start measurement press

`START/STOP`

During the measurement, the following error or status messages may occur:

Message	Comment
FKT : no INFO2 det.	No INFO2 received.
FKT : no INFO4 det.	No INFO4 received
FKT : INFO0 det.	INFO0 received.
FKT : undef. INFO !	No defined INFO was received.
FKT : permanent ZERO	Binary "0" in the data channels
FKT : AIS	Binary "1" in the data channels
FKT : BITSLIP	Bit change in the data
FKT : LAYER 1 ERROR	Layer 1 error
FKT : wrong Amplitude	Receiver amplitude too large or too small.
MEASUREM. aborted	Measurement aborted.
FKT: WAITING	Message during synchronizing process on NT
WAITING 4 LOOPBACK	Waiting for the reception of the data.

If layer 1 cannot be activated or remains activated at the test object, the following messages are displayed alternately:

```
FKT : LAYER 1 ERROR
```

```
MEASUREM. aborted
```

If you want to start a new measurement, e.g. after correcting a test object error, the following key must be pressed twice:

```
START/STOP
```

Results display

The measurement results are displayed in the following form:

BE :	Count		Count of bit error counter; max 2^{32}
TIME:	Count	s	Count of seconds passed; max 2^{32}
BER:	Bit error rate	BE/s	Continuously calculated bit error rate; is deleted at the end of the set gate time and regenerated.
Conformance	TRUE/FALSE/INC.		Is set to TRUE after the first error-free gate time has expired
Int. :	Count		Total of measured gate times (interval)
err. Int.:	Count		Total of measured gate times with bit errors

5.2.3 Receiver Input Delay Characteristics

(A.8.6.3.-ETS300 012)

The sensitivity of the NT receiver to the cycle delay is registered with a bit error measurement. The measurement process corresponds to the one of Receiver sensitivity.

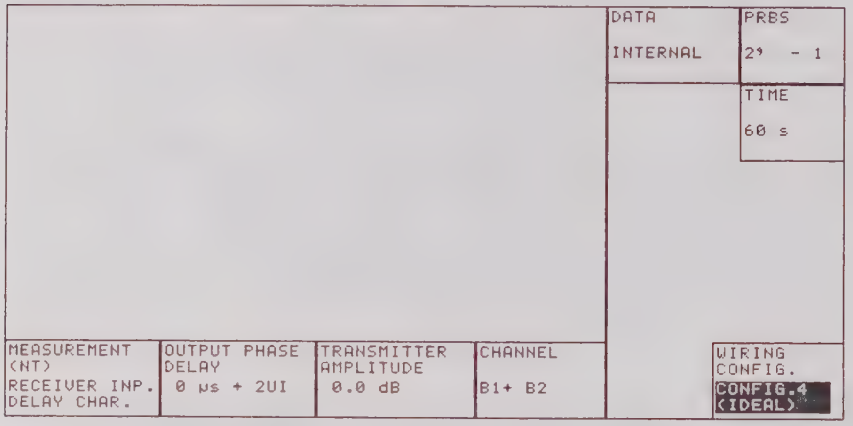
According to the CCITT recommendations, there are four different bus configurations. If the Artificial Line Option 7KK1403-2AA (add-on-board for K1403) is connected, the signal is not only attenuated but also delayed (delay time) and distorted (skin effect). The cycle delay can be adjusted from -8µs to +35µs in increments of 1µs. Additionally, the transmitted amplitude can be adjusted from -8 dB to +3 dB in increments of 0.1 dB. The network terminator NT to be tested must not generate any bit errors during 1 minute.

Required are:

Condition on NT	Clause / subclause	Configuration	Round trip delay
For short passive bus	A.8.6.3.1	ii and iii	10 to 14µs
For point-to-point and passive bus	A.8.6.3.2	i ii and iii	10 to 42µs 10 to 13µs
For extended bus	A.8.6.3.3	see note	10 to 42µs
For point-to-point	A.8.6.3.4	i	10 to 42µs
Note : This configuration consists of a cable having a characteristic impedance of 75 ohms, a capacitance of 120nF/km, a loss of 3.8dB at 96kHz, four TEs connected such that the differential delay of signals from different TEs is in the range of 0 to 2µs			

During the test a PRBS signal is transmitted and the bit error count BEC and the bit error rate BER are measured at the test object with a loop switched on or at the LT simulation to be used. Since this measuring mode according to ETS is assigned to the measurement of electrical characteristics of an NT, it is selected via the menu ELECTRICAL CHARACTERISTICS ON NT.

Measuring mode Receiver Input Delay Characteristics



Setting parameters (MENU)

MESSART
IMPEDANCE
UNBALANCE
PULSE SHAPE
TRANSM. OUTP. IMP. ACTIVE
OUTPUT PEAK CURRENT
JITTER
RECEIVER SENSITIVITY
RECEIVER INP. DELAY CHAR.

FRAME DELAY	TRANSMIT. AMPLITUDE	CHANNEL	DATA	PRBS
EDIT	EDIT	B1	INTERNAL	2^9-1
0 µs + 2UI	-1.5dB	B2	EXTERNAL	2^{11}-1
	0dB	B1+B2		2^{15}-1
	+1.5dB			2^{20}-1

TIME	WIRING CONFIG.
EDIT	FREE CONFIG.
60s	CONFIG. 1
	CONFIG. 2
	CONFIG. 3a
	CONFIG. 3b
	CONFIG. 4 (IDEAL)

The *wiring configuration* is realized via the **Artificial Line Option**.

ARTIFICIAL LINE OPTION

Dependencies

DATA	
INTERNAL	EXTERNAL
PRBS	---
2^9-1	---
2^{11}-1	---
2^{15}-1	---
2^{20}-1	---

If you select the internal source for the data to be transmitted, one of four different pseudo-random sequences can be selected. The parameter PRBS is thus dependent on the selection of the parameter DATA INTERNAL/EXTERNAL. If you select DATA EXTERNAL, an external source can be coupled to the sockets BU2 to BU4 on the front of the unit. A statement about the number of bit errors and the bit error rate is not possible in this case. Therefore, the values remain on 0 during the measurement and the conformance result is set to INCONCLUSIVE.

To start measurement press

START/STOP

During the measurement, the following error or status messages may appear:

Meldung	Kommentar
FKT : no INFO2 det.	No INFO2 received.
FKT : no INFO4 det.	No INFO4 received.
FKT : INFO0 det.	INFO0 received.
FKT : undef. INFO !	No defined INFO was received.
FKT : permanent ZERO	Binary "0" in the data channels
FKT : AIS	Binary "1" in the data channels
FKT : BITSLIP	Bit change in the data
FKT : LAYER 1 ERROR	Layer 1 error
FKT : wrong Amplitude	Receiver amplitude too large or too small.
State Intchg. -> G2	State interchange from G3 (INFO4 recd.) to G2 (INFO2 recd.)
MEASUREM. finished	Measurement finished
MEASUREM. aborted	Measurement aborted.
WAITING 4 LOOPBACK	Waiting for the reception of the data.

If layer 1 cannot be activated or remains activated at the test object, the following messages are displayed alternately:

```
FKT : LAYER 1 ERROR
```

```
MEASUREM. aborted
```

If you want to restart the measurement, e.g. after correcting a test object error, press the following key twice:

```
START/STOP
```

Presentation of results

The measuring results are presented in the following form:

BE :	Count		Count of bit error counter; max 2^{32}
TIME:	Count	s	Count of seconds passed; max 2^{32}
BER:	Bit error rate	BE/s	Continuously calculated bit error rate; is deleted at the end of the set gate time and regenerated.
Conformance	TRUE/FALSE/INC.		Is set to TRUE after the first error-free gate time has expired.
Int. :	Count		Total of measured gate times (interval)
err. Int.:	Count		Total of measured gate times with bit errors

SIEMENS

ISDN S_0 Analyzer K1403

S0 Artificial Line

User Manual C73000-B6076-C65-2

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CE

The product described in this manual complies with the statutory regulations on electromagnetic compatibility of devices (EMC) or the regulations of the guideline of the council from 03.05.1989 for adaptation of the statutory regulations of the member countries on electromagnetic compatibility of devices (89/336/EEC).

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1 Safety information

The ISDN S_0 Analyzer K1403 has been constructed and tested in accordance with Publication EN61010 Safety Provisions for Electronic Measuring Equipment Safetyand has left the factory in a perfectly safe condition. In order to maintain optimum safety and ensure hazard-free operation, please adhere to the following basic rules.

- Transport the device only in its original packing or by using the transport case specially recommended for the K1403. This will protect the device against shocks.
- The K1403 is exclusively intended for indoor use. Condensation may occur when the unit is brought to its site of operation from a cold environment. Operation is only permissible with an absolutely dry unit after its temperature has adjusted to the environment.
- Before implementing and operating the K1403, make sure that the environmental conditions are complied with. The environmental conditions Environmental conditionsare listed under the heading "Technical data" in the appendix.
- Before switching on the device, make sure that the preset operating voltage Operating voltageof the device corresponds to the permissible line voltage.
- Make sure that replacement fuses are of the specified type and rating: Use 3.15 A/250V (type T) fuses.
- The power plug must only be inserted into a grounded socket. Do not cancel the protective effect by using an extension cable without a protective ground conductor.
- Make sure that the ventilation slots on the rear and top of the device are not covered.
- The unit can become dangerous if the protective ground conductor is interrupted either inside or outside the unit. Do not interrupt the protective ground conductor intentionally. The same applies when loosening the connection for the protective ground conductor. When opening covers or removing parts, remember that live parts may be exposed if the unit is connected. Connection points may also be live. Disconnect the unit from all voltage sources prior to adjustment, maintenanceMaintenance, repair or when replacing parts. If such work on live and open units cannot be avoided, it should only be performed by qualified staff familiar with the hazard involved.

- All modules contain electro-sensitive components. Please note the necessary precautions and ESD safety measuresESD safety measures:

Warning!

When electrical devices are in operation certain parts of these device are live. Non-observance of the above precautions may therefore lead to severe physical injuries or to serious material damage.

Only qualified staff may handle this device or work in its vicinity. They must be thoroughly familiar with all the warnings, safety and maintenance information contained in these instructions. Faultless and safe operation of the device presupposes proper transport, proper storage, set-up and mounting as well as careful handling and servicing.

2 Device description

2.1 S_0 Artificial line

The module Artificial Line includes the following functions:

- Simulation of high-capacitive cable (120 nF/km) up to 1 km length
- Simulation of low-capacitive cable (30 nF/km) with 200 m length
- Noise generator for symmetrical noises
- TE loads (1 to 7 TEs)
- 100 Ω terminating resistors
- S_0 transformer
- RJ45 sockets (see description of sockets)

Design and mode of operation

The Artificial Line is switched as a bus configuration between the measuring unit and the IUT (ITEM UNDER TEST). The possible combinations and the definition of terms in the menu are shown in the overview.

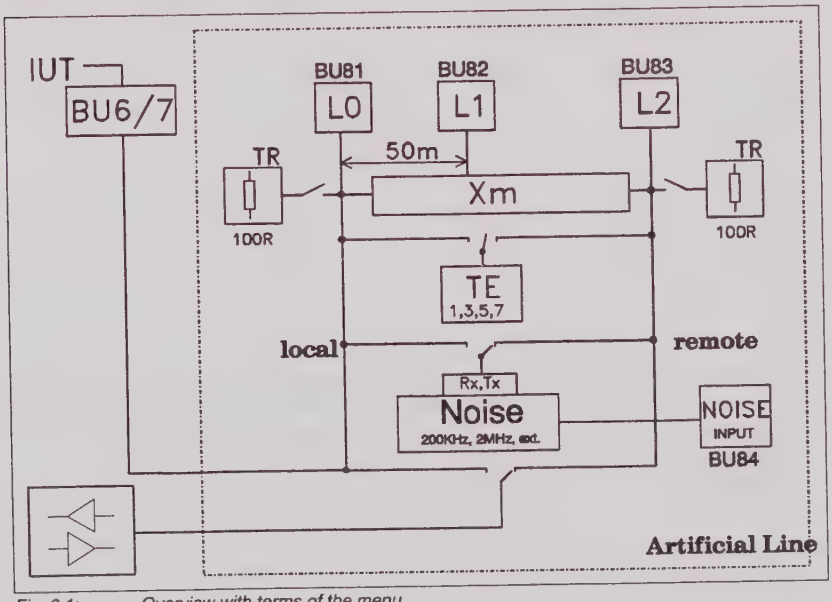


Fig. 2.1: Overview with terms of the menu

In order to test the functionality and conformity of the terminal units and the mains terminal units relative to the transmission medium, various measurements are defined according to ITU-T-rec. I430[1], which require two different simulations of a balanced pair cable. One is the high-capacitive line with a capacitance per unit length 120 nF/km and the other a low-capacitive line with 30 nF/km. Thus all test

[1] formerly CCIT I.430

ITU: International Telecommunication Union

configurations are switchable which are described in the recommendations ITU-T-rec. I430 Annex D.

The Artificial Line can be switched on for the following measuring modes defined in ITU-T-rec. I430, ETSI 300012[2] and CTS-2-ISDN[3].

a) Jitter

b) Frame delay

c) Receiver sensitivity

d) Basic interconnection test (defined only in CTS-2-ISDN)

See also:

a) Measuring modes Jitter and Frame delay in the manual K1403

b) Measuring modes Receiver sensitivity and Basic interconnection test in the description of the "Functional Test" module

[2] ETSI: European Telecommunications Standards Institute

[3] CTS: Conformance Testing Services

Line module

The line simulation consists of a series connection of several modules each of which simulates a cable of 50 m length. All modules are constructed identically and consist of a balanced network with closely toleranced components. Thus attenuation, delay and wave impedance of the cable are exactly simulated within a frequency range from DC to 1 MHz.

The line modules have the following specifications: (at 96 kHz)

Capacitance per unit length	C'	=	120 nF/km (HC[4])
	C'	=	30 nF/km (LC[5])
Resistance per unit length	R'	=	160 Ω/km (HC)
	R'	=	160 Ω/km (LC)
Wave impedance	Zw	=	75 Ω (HC)
	Zw	=	150 Ω (LC)

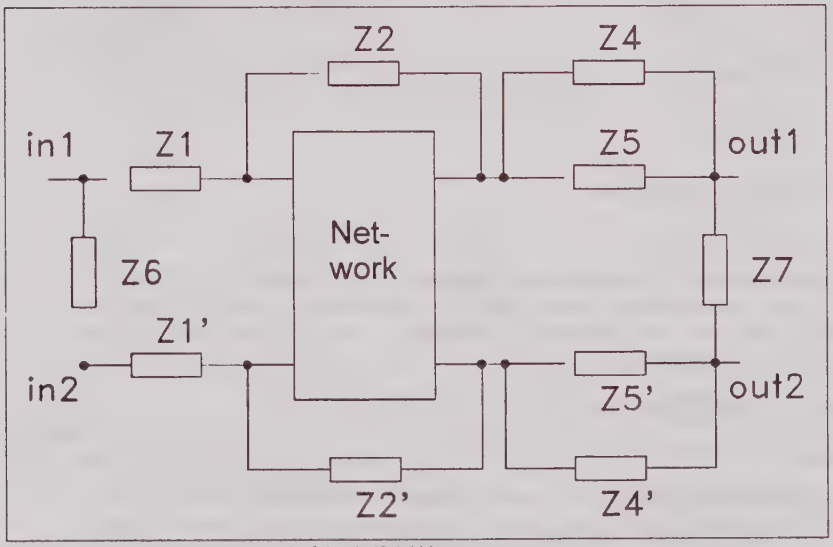


Fig. 2.2: A submodule (25 m) of the Artificial Line

[4]HC: high capacity

[5]LC: low capacity

Noise generator

The noise generator is used to couple an isolated symmetric noise voltage into the Artificial Line via high-resistance coupling.

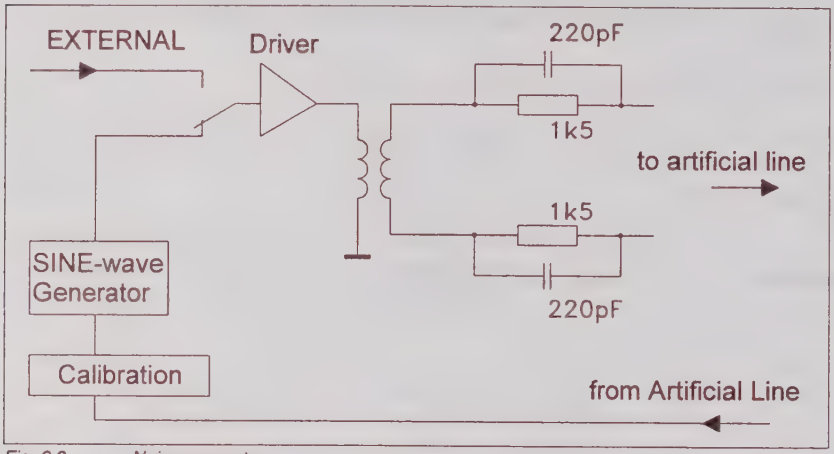


Fig. 2.3: Noise generator

There are three operating modes:

External noise

In this operating mode a signal injected via the external socket NOISE (BU84) is amplified by the line driver and coupled with high resistance (= current source) into the Artificial Line via the transmitter. A voltage of 20 V_{pp} may apply at the transmitter in secondary circuit.

The level of the external source should not rise above ± 0,75 V.

200 kHz SINE

The built-in sine-wave generator delivers a sinusoidal signal with 100 mV_{pp} and a frequency of 200 kHz at the coupling point. To ensure this amplitude for all possible loads at the S_0 bus, the generator is calibrated internally and automatically via a "Calib" signal. During the calibration process no other transmitter may apply to the bus (see note in chapter 4.3).

2 MHz SINE

Same as 2., but with 2 MHz SINE

Frequency stability of oscillator 1-7 TEs: ± 50 ppm

Setting tolerance of amplitude 1-7 TEs: ± 10%, configuration 1, 3a, 3b
± 25%, configuration 2

TE loads

The impedance characteristic of a TE is simulated with a passive network. This corresponds to the impedance characteristic described in "Appendix A1 CTS-2 Test requirements" for one or several TEs respectively.

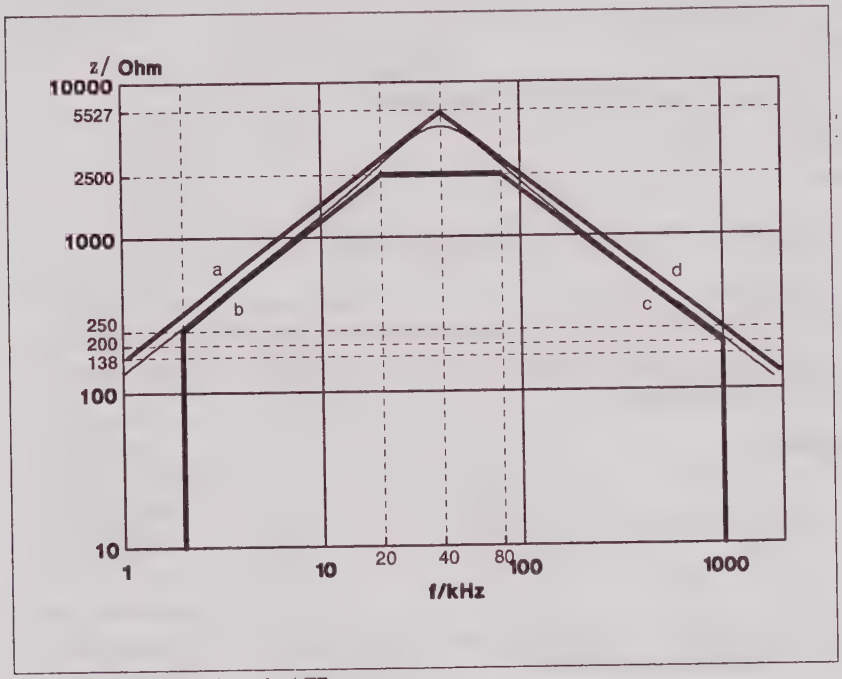


Fig. 2.4: TE-impedance for 1 TE

a Slope = 22mH, b Slope = 20 mH, c Slope = 800pF, d Slope = 720 pF
The impedance behavior is calculated and implemented in accordance with the above-mentioned characteristic.

Terminating resistors/S_0 transmitters/RJ45 sockets

The prescribed terminating resistors of 100 Ω ± 1% can be switched via relays onto the beginning or end of the line. The S_0 transmitters form the connection of the measuring modules of the K1403 to the simulated bus. The RJ45 sockets (BU81-BU83) which are positioned at the rear wall of the module allow access to the S_0 bus at three different points.

a) 0 m (beginning of line)

b) 50 m

c) 100...1000 m (end of line)

Noise generator

The noise generator is used to couple an isolated symmetric noise voltage into the Artificial Line via high-resistance coupling.

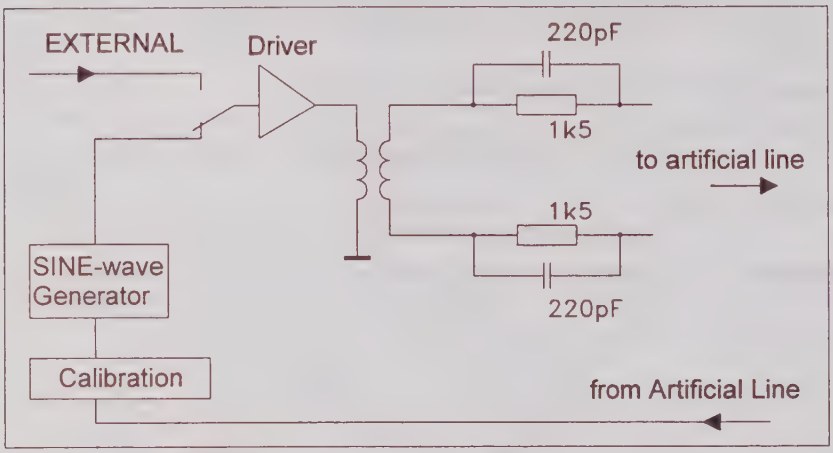


Fig. 2.3: Noise generator

There are three operating modes:

External noise

In this operating mode a signal injected via the external socket NOISE (BU84) is amplified by the line driver and coupled with high resistance (= current source) into the Artificial Line via the transmitter. A voltage of 20 V_{pp} may apply at the transmitter in secondary circuit.

The level of the external source should not rise above ± 0,75 V.

200 kHz SINE

The built-in sine-wave generator delivers a sinusoidal signal with 100 mV_{pp} and a frequency of 200 kHz at the coupling point. To ensure this amplitude for all possible loads at the S_0 bus, the generator is calibrated internally and automatically via a "Calib" signal. During the calibration process no other transmitter may apply to the bus (see note in chapter 4.3).

2 MHz SINE

Same as 2., but with 2 MHz SINE

Frequency stability of oscillator 1-7 TEs:	± 50 ppm
Setting tolerance of amplitude 1-7 TEs:	± 10%, configuration 1, 3a, 3b ± 25%, configuration 2

TE loads

The impedance characteristic of a TE is simulated with a passive network. This corresponds to the impedance characteristic described in "Appendix A1 CTS-2 Test requirements" for one or several TEs respectively.

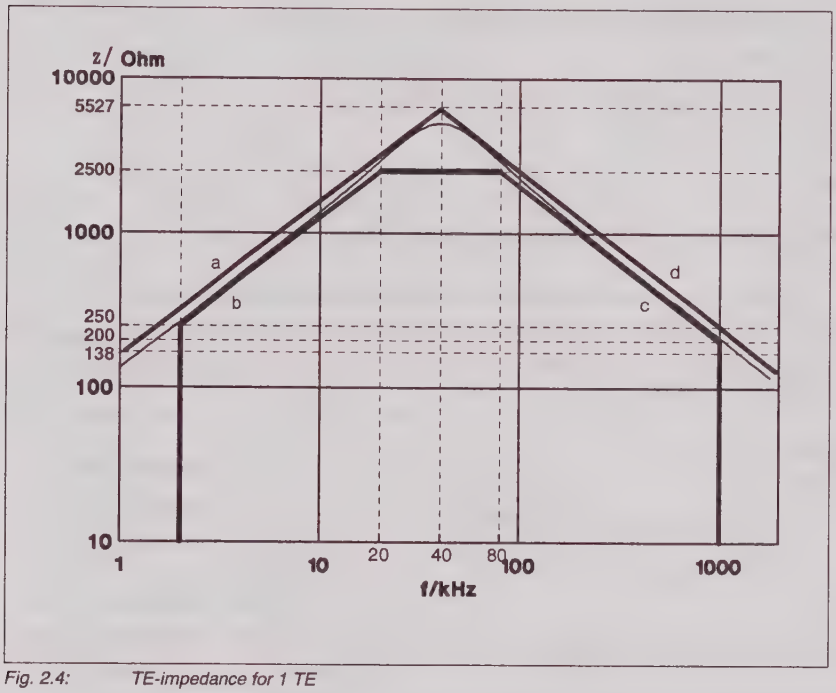


Fig. 2.4: TE-impedance for 1 TE

a Slope = 22mH, b Slope = 20 mH, c Slope = 800pF, d Slope = 720 pF
The impedance behavior is calculated and implemented in accordance with the above-mentioned characteristic.

Terminating resistors/S_0 transmitters/RJ45 sockets

The prescribed terminating resistors of 100 Ω ± 1% can be switched via relays onto the beginning or end of the line. The S_0 transmitters form the connection of the measuring modules of the K1403 to the simulated bus. The RJ45 sockets (BU81-BU83) which are positioned at the rear wall of the module allow access to the S_0 bus at three different points.

a) 0 m (beginning of line)

b) 50 m

c) 100...1000 m (end of line)

Possible configurations

Figs. 5 to 9 give a schematic overview of the possible configurations and their adjustments via relays. The Artificial Line (case with Xm) can be switched for the following lengths:

- 100 m ...200 m (default: 100 m ≙ 1 µs delay [6]
- 500 m
- 600 m
- 650 m ...750 m (default: 750 m ≙ 6 dB attenuation [7]
- 800 m
- 900 m
- 1000 m

Both lengths can be changed on the module with jumpers (see jumper overview, Chapter 7.2).

Via the RX-DIRECT relay the RX pair wire can be looped through ideally (without Artificial Line = 0 m) from the IUT to the measuring module in the K1403.

The switching options were selected in such a way that all bus configurations required in the ITU are possible.

Configuration 1

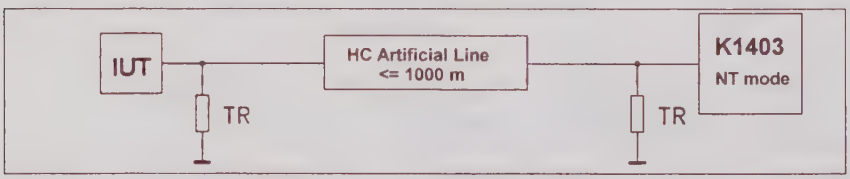


Fig. 2.5: Point to point (Configuration 1)

System attenuation 6 dB, 120 nF/km cable, length ≤ 1000 m, load: IUT

Setting of Artificial Line

Fixed setting parameters according to ITU

- Length of line: 650...750m (6 dB)
- Noise type: TX
- TE configuration: Off
- TR remote: On
- K1403 ON: Remote

[6] The length for 1 µs delay (delay for one direction. This corresponds to a "round trip delay" of 2µs) equals
100 m and corresponds to the delay time for the short passive bus required in ITU-T-rec.I430.

[7] The length for 6 dB attenuation is 750 m and corresponds to the line with 6 dB attenuation at 96 kHz required in the ITU-T-rec.I430.

Variable setting parameters

- Noise frequency: Off / 200 KHz / 2 MHz / external
- Noise distance: Local / remote
- TR local: On / off

Configuration 2

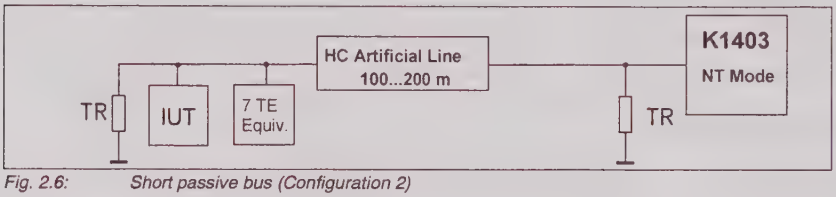


Fig. 2.6: Short passive bus (Configuration 2)

Signal delay of the unloaded cable 1 µs, 120 nF/km cable, length 100...200 m, load: IUT+7TE

Setting of the Artificial Line

Fixed setting parameters according to ITU

- Length of line: 100...200m (1 µs)
- Noise type: TX
- TE configuration: Local
- TE number: 7 TE
- TR remote: On
- K1403 ON: Remote

Variable setting parameters

- Noise frequency: Off / 200 KHz / 2 MHz / external
- Noise distance: Local / remote
- TR local: On / Off

Configuration 3a

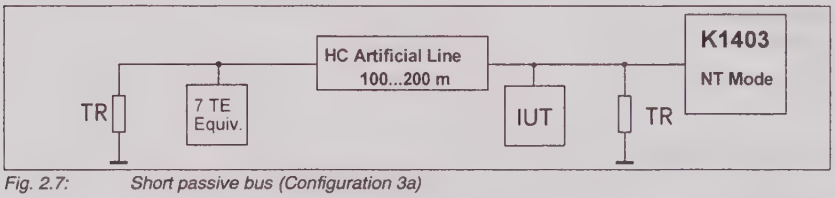


Fig. 2.7: Short passive bus (Configuration 3a)

Signal delay of the unloaded cable 1 µs, 120 nF/km cable, length 100...200 m, load: 7TE+IUT

Setting the Artificial Line

Fixed setting parameters according to ITU

- Length of line: 100...200m (1 μs)
- Noise type: TX
- TE configuration: Remote
- TE number: 7 TE
- TR local: On
- K1403 ON: Local

Variable setting parameters

- Noise frequency: Off / 200 KHz / 2 MHz / external
- Noise distance: Local / remote
- TR-FERN: On / Off

Configuration 3b

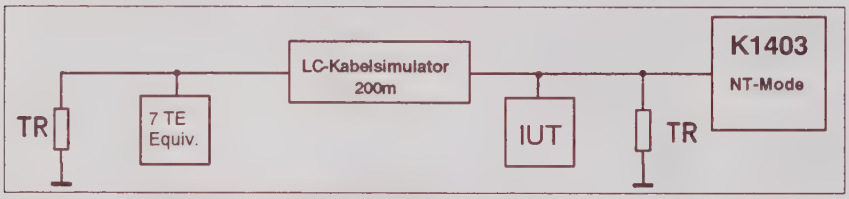


Fig. 2.8: Short passive bus (Configuration 3b)

Signal delay of the unloaded cable 1 µs, 30 nF/km cable, length 200 m, load: 7TE + IUT

Setting the Artificial Line

Fixed setting parameters according to ITU

- Length of line: 100...200m (1 μs)
- Noise type: TX
- TE configuration: Remote
- TE number: 7 TE
- TR local: On
- K1403 ON: Local

Variable setting parameters

- Noise frequency: Off / 200 KHz / 2 MHz / external
- Noise distance: Local / remote
- TR remote: On / Off

Configuration 4

(ideal)

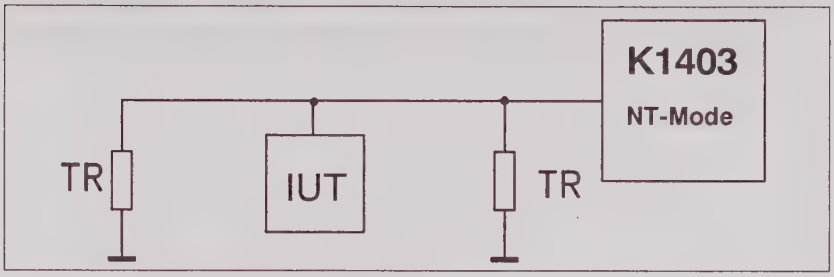


Fig. 2.9: Ideal configuration (Configuration 4)

Except for the S_0-bus terminals (TR), none of the parameters can be set.

Extendended passiv bus

(only by isolated cable simulator)

The settings of the configuration is conform to ITU-T-rec. I430.

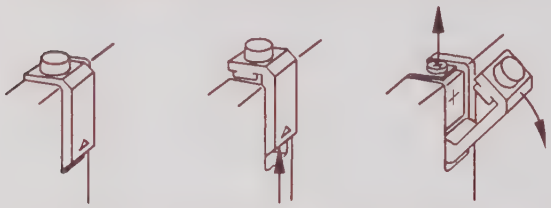
3 Start-up preparations

The following pages will tell you how to make the ISDN S_0 Analyzer ready for use. It will also tell you what you must observe when mounting the K1403 modules.

3.1 Mounting a module

First, remove the cover of the device. The fixing screws for the cover are covered by four corner latches. Proceed as follows:

➤ Push the corner latches some 4 mm upward in direction of the arrow until you meet resistance and unhinge the corner latches.



➤ Loosen the four screws which are now accessible and remove the cover.

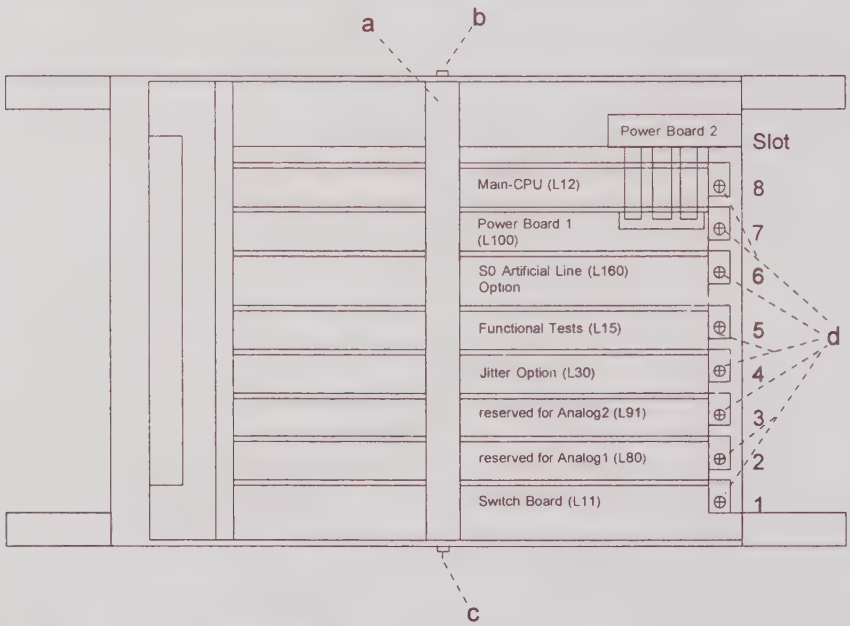


Fig. 3.1: Set-up of the modules

➤ Take the support (a) out by removing screws (b) and (c).

➤ Loosen the module slot screw (d). Insert the module into its destined slot. Ensure that it is correctly assigned and properly fitted in the guide support.

➤ Tighten the module slot screw (d). Re-mount the support (a). Position the printed board in the grooves of the support and tighten screws (b) and (c).

➤ Re-attach the cover of the device.

4 Operation

The required measuring mode, the test parameters and all equipment parameters are clearly arranged on a large, self-luminous electroluminescent display and set with the aid of operator prompting (menu technique).

Operator prompting is performed with selection windows and interactively changing softkey combinations. Functions or parameters are selected by simply touching the relevant part of the touch screen. No pressure needs to be exerted. Each selection is acknowledged by inversion and is implemented when the panel is exited.

If several setting parameters are offered, these are combined into a single selection window. This window appears after the parameter, e.g. transmitted level has been selected and is deleted after a value has been selected.

There are only two menu levels: the basic menu (which appears after switch-on) and the working menu. The latter is actively adapted, i.e. expanded or simplified, to the given setting or operating mode (START, STOP, RESULT).

Only those touch panels which are necessary or expedient for an application are faded in. Other possibilities need not be taken into account.

4.1 Control elements and sockets

RJ45 sockets

(see fig. 11 and Operating instructions ISDN S_0 Analyzer for pin assignment)

BU81 (L0)

Connection to the simulated S_0 BUS close to the IUT

BU82 (L1)

Connection to the simulated S_0 BUS 50 m away from the IUT

BU83 (L2)

Connection to the simulated S_0 BUS Xm away from the IUT (Xm = length setting selectable via menu)

BNC socket

BU84 (NOISE)

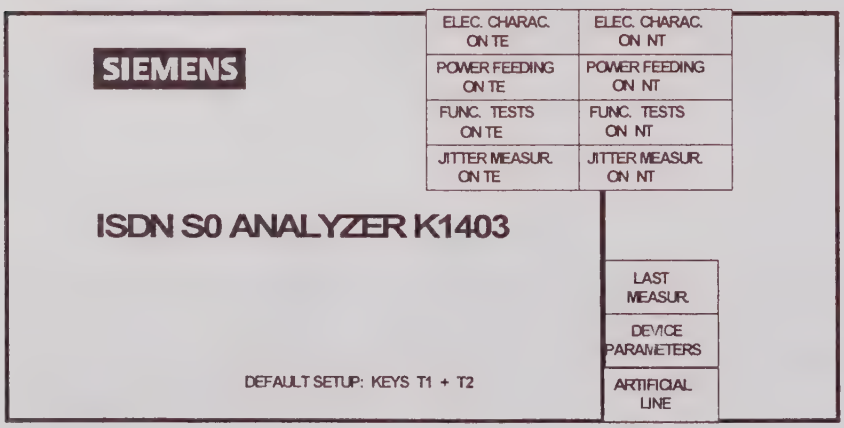
Connection possibility of an external noise generator
Input impedance: 75 Ω
Input amplitude: $V_{in} \leq 1.5\ V_{pp}$

Fig. 4.1: Pin assignment of the RJ45 sockets

Supply voltage	Signal	RJ45 socket
+ U_F [8]	S_{REC1} (+)	3
+ U_F [1]	S_{REC2} (-)	6
- U_F [1]	S_{TRX1} (+)	4
- U_F [1]	S_{TRX2} (-)	5

Signal switch for NT according to FTZ 1TR230, 386TR2 and T1D1

4.2 Summary of operation



[8] Polarity for normal operation. In case of emergency operation, (+) and (-) are interchanged.

5 Measurement and presentation of results

5.1 Line configuration TE

					TE CONFIG. FAR	NUMBER OF TE'S 1 TE
					TR NEAR ON	TR FAR ON
					K1403 AT REMOTE	RX DIRECT OFF
LINE CONFIG. FREE CONFIG.	WIRING LENGTH 100 ... 200 m (2 µs)	NOISE FREQUENCY OFF	NOISE DISTANCE NEAR	NOISE TYPE TX		RETURN

Table of key assignments

LINE CONFIG.:	LINE LENGTH	NOISE-FREQUENCY	NOISE DISTANCE	NOISE TYPE
FREE CONFIG.	100.. 200m (2µs)	OFF	REMOTE	RX
CONFIG. 1	500m	200kHz	LOCAL	TX
CONFIG. 2	600m	2MHz		
CONFIG. 3A	650.. 750m (6dB)	EXTERNAL		
CONFIG. 3B	800m			
CONFIG. 4	1000m			

TE CONFIG:	TR NEARL	K1403 AT	NUMBER OF TE'S	TR FAR	RX DIRECT
OFF	OFF	REMOTE	1 TE	OFF	OFF
REMOTE	ON	LOCAL	3 TEs	ON	ON
LOCAL			5 TEs		
			7 TEs		

Presentation of results

See measuring modes jitter or frame delay in **Operating instructions K1403 ISDN S_0 Analyzer.**

Setting parameters

`Line configuration`

Switch Artificial Line off (OFF) or on (FREELY SELECTABLE)

`Length of line`

Setting total length of line

`Noise frequency`

Selection of noise (none, external, 200 kHz or 2 MHz sine)

`Noise distance`

Coupling of noise to line, local or remote from IUT

`Noise type`

Defines the pair wire into which noise is coupled

`TE configuration`

Coupling of TE simulators local or remote from IUT

`TE number`

Possible settings of TE simulator of 1, 3, 5, 7 TEs

`TR local, remote`

Terminating resistors may be switched local or remote from IUT

`K1403 ON`

Coupling of measuring modules into K1403 local or remote from IUT

`RX DIRECT`

Ideal jumpering of RX pair wires (ON = IDEAL connection, OFF = RX pair wire via Artificial Line)

The current setting is displayed in the menu. If LINE CONFIGURATION OFF is selected the IUT is in any case ideally connected with the measuring modules. Then no setting in the menu line configuration has any influence on the measurement.

It must be ensured that after the start of a measurement with the sine noise generator no unit transmits on the interfered pair wires as long as the noise generator calibrates.

For the NT measurement, for example, this means that TEs applying to the bus can only transmit in INFO0.

6 Appendix

The following pages contain the Technical Data for the artificial line. Following these pages, you will find the measurement characteristics and jumper positions. Furthermore, there is information on how the artificial line is to be used at the basic terminal.

6.1 Technical specifications

The high-capacitive Artificial Line has variable length settings up to a maximum of 1000 m. It consists of a series connection of several modules each of which simulates a cable of 50 m length. All modules are constructed identically and consist of a balanced network with closely toleranced components. Thus, attenuation, delay and wave impedance of the high-capacitive cable are exactly simulated within a frequency range of DC up to 1.0 MHz.

The technical specifications of the **HC** Artificial Line are:

Wires	n	= 4	
Line diameter	Φ	= 0.6 mm	
Cable length	L	= 1000 m	
Frequency	f	= DC - 1.0 MHz	
Capacitance per unit length	C'	= 120 nF/km ± 5%	typically, calculated
Resistance per unit length	R0' (DC) R' (96 kHz)	= 130 Ω / km ± 5% = 160 Ω / km ± 5%	typically, calcul.
Terminating resistor 100 Ω	Ω	= 100 ± 3 %	
Conductance per unit length	G'	galvanically separated	
Wave impedance	Zw (96 kHz)	= 78,8 Ω ± 5%	
TE loads		are connected internally	
Attenuation Group delay	a1 (750m) trgo (100m)	- 6.0.....-6.2 dB 930.....950 ns	
Noise generator 200 kHz, 2Mhz	dB	-26,8 ± 0,7dB	
Max. allowance curr.	Imax	= 200 mA	
Max. voltage between wires	Umax	= 60 V	

The low-capacitive Artificial Line has a fixed length of 200 m. It also consists of a series connection of 50 m modules.

The technical specifications of the **LC** Artificial Line are:

Wires	n	= 4	
Line diameter	Φ	= 0.6 mm	
Cable length	L	= 200 m	
Frequency	f	= DC - 1.0 MHz	
Capacitance per unit length	C'	= 30 nF/km ± 5%	typically, calculated
Resistance per unit length	R0' (DC) R' (96 kHz)	= 130 Ω / km ± 5% = 158 Ω / km ± 5%	typically, calcul.
Terminating resistor 100 Ω	Ω	= 100 ± 3 %	
Conductance per unit length	G'	galvanically separated	
Wave impedance	Zw (96 kHz)	= 149 Ω ± 5%	
TE loads		are connected internally	
Attenuation Group delay	ao (200m) trgo (200m)	- 7.2.....-7.5 dB 990.....1010 ns	
Noise generator 200 kHz, 2Mhz	dB	-26,8 ± 0,7dB	
Max. allowable current	Imax	= 200 mA	
Max. voltage between wires	Umax	= 60 V	

6.2 Measurement curves

All measurement curves were recorded with a symmetrical level transmitter and a symmetrical probe. The measuring switch and the probe are shown below:

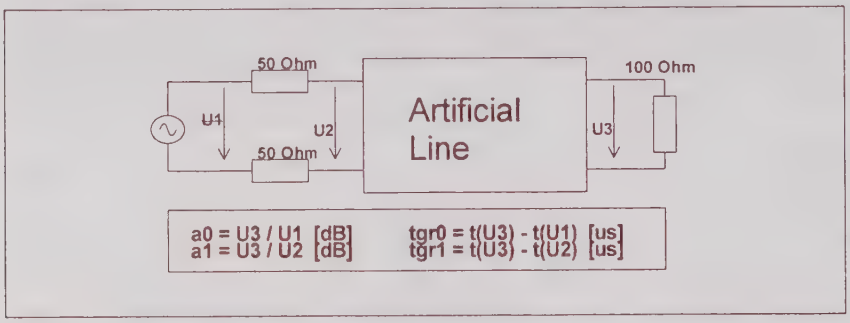


Fig. 6.1: Measuring switch

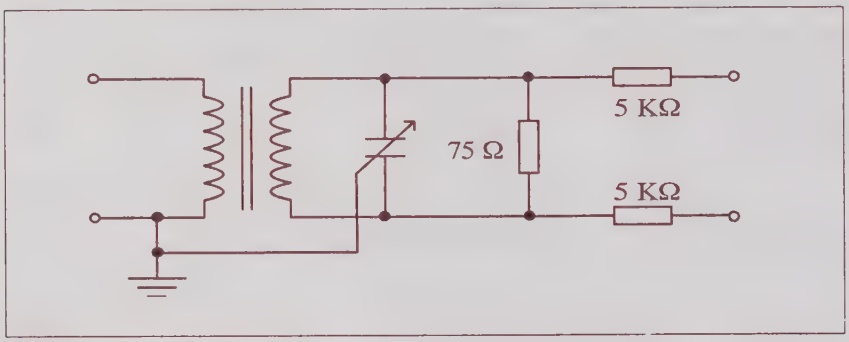


Fig. 6.2: Symmetrical probe

Measurement curves for the high-capacitive Artificial Line

Attenuation and group delay for all length settings:

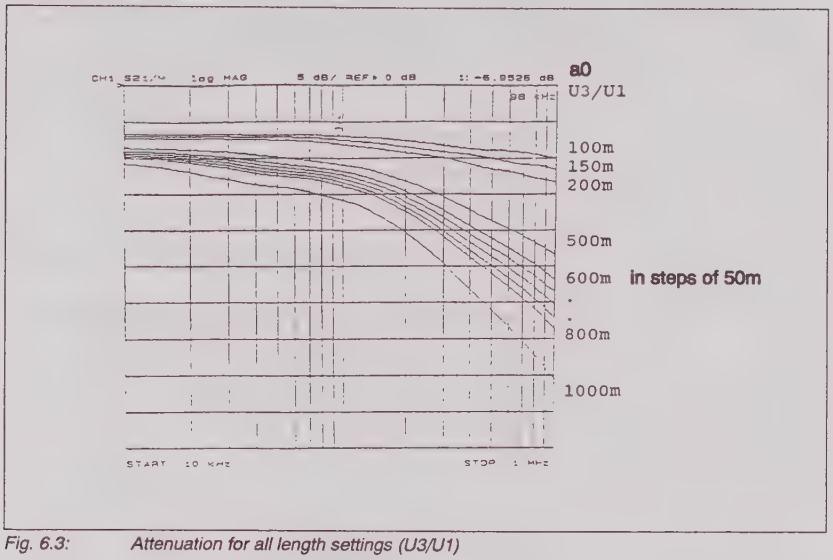


Fig. 6.3: Attenuation for all length settings (U3/U1)

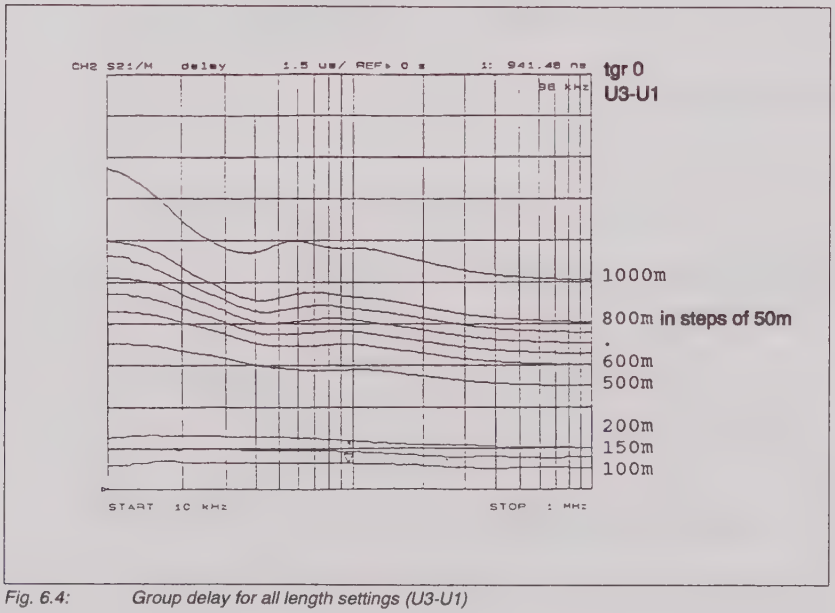


Fig. 6.4: Group delay for all length settings (U3-U1)

Attenuation and group delay for 1 µs line:

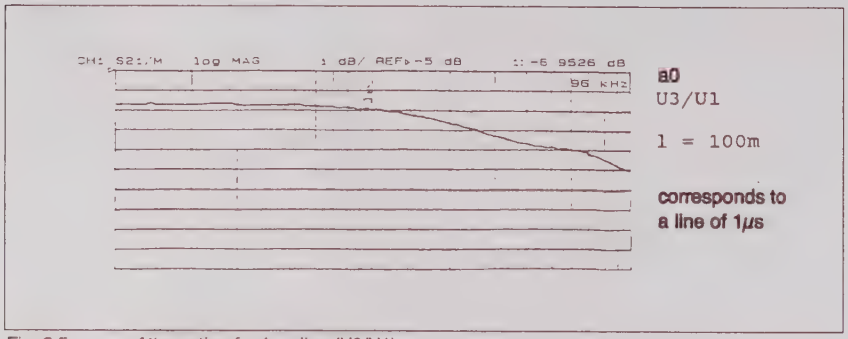


Fig. 6.5: Attenuation for 1 µs line (U3/U1)

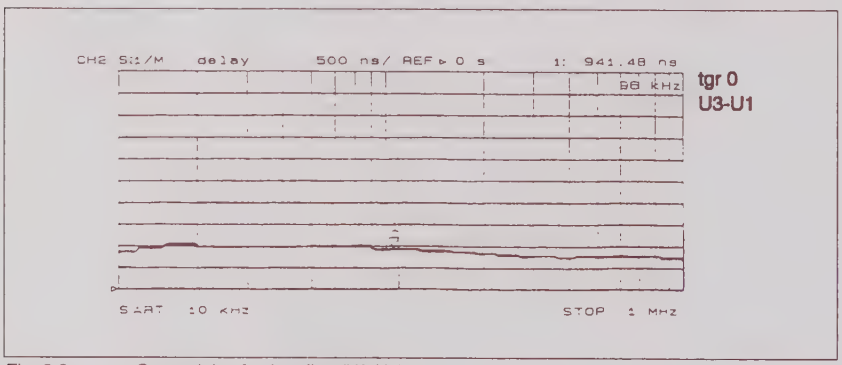


Fig. 6.6: Group delay for 1 µs line (U3-U1)

Attenuation and group delay for 6 dB line

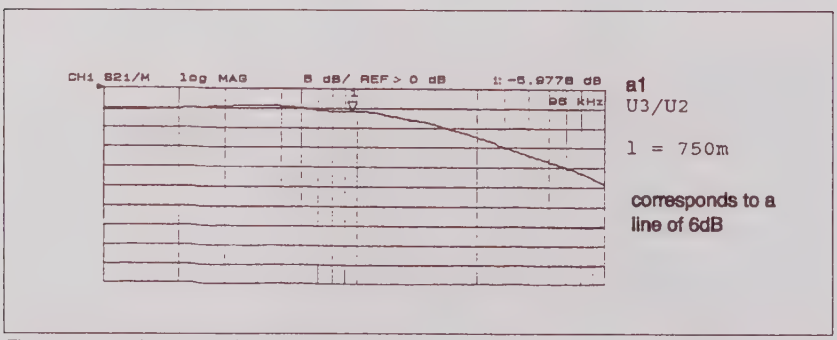


Fig. 6.7: Attenuation for 6 dB line (U3/U2)

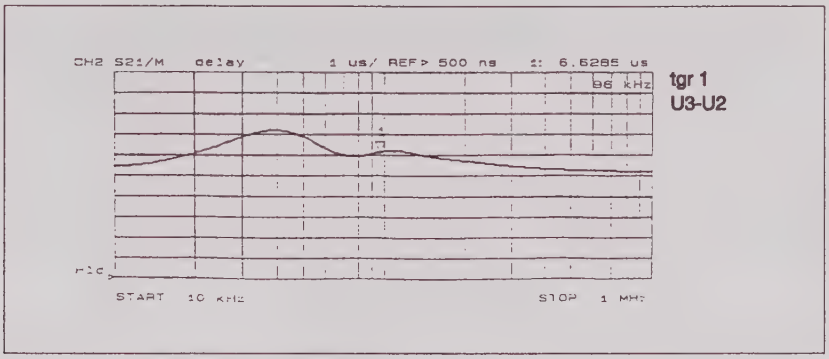


Fig. 6.8: Group delay for 6 dB line (U3-U2)

Wave impedance magnitude and phase (nominal value from computer simulation)

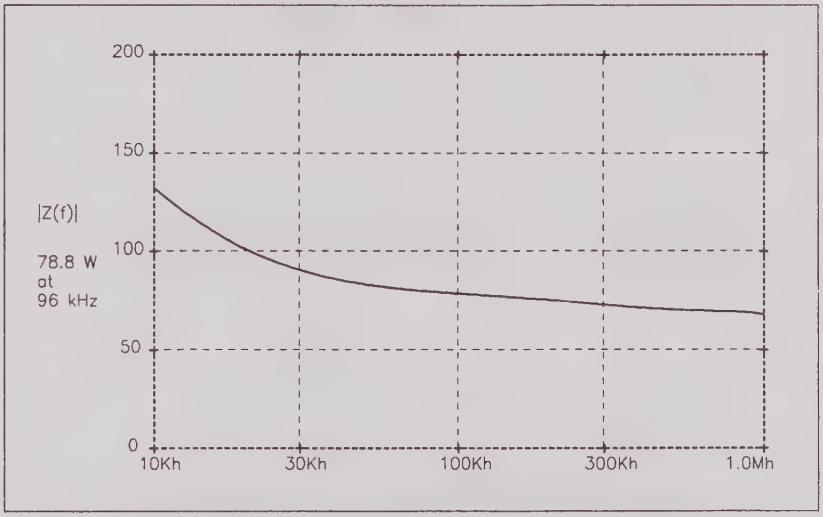


Fig. 6.9: Magnitude of wave impedance

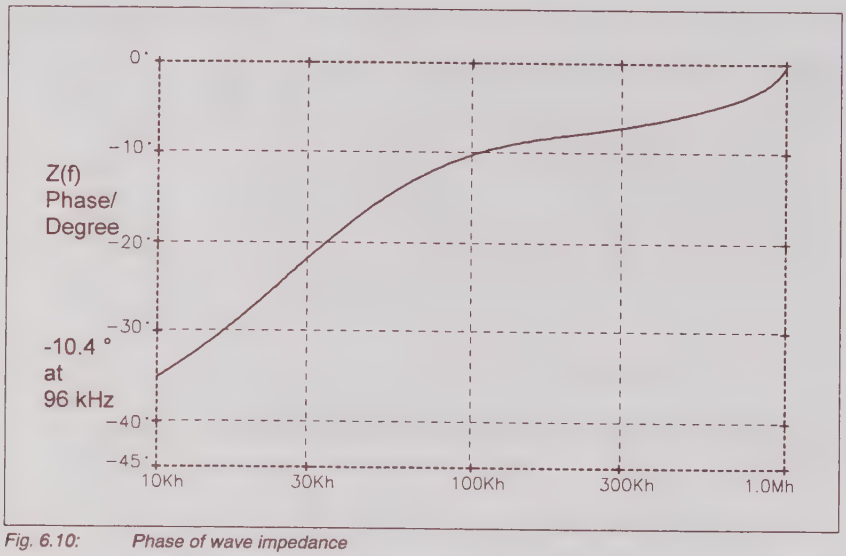


Fig. 6.10: Phase of wave impedance

During all measurements on the Artificial Line, the measuring instruments must be balanced to earth. The curves were measured without the S_0 transmitter on the module.

Measurement curves for the low-capacitive Artificial Line

With a line length of 200 m and the activated terminating resistors (TR=100 Ω), the signal delay of the fundamental wave equals

tgr0 (96 kHz) = 0.96 µs

The attenuation of the simulated line for the fundamental wave equals

a0 (96kHz) = 7.4 dB ; a1 (96kHz) = 3.1 dB

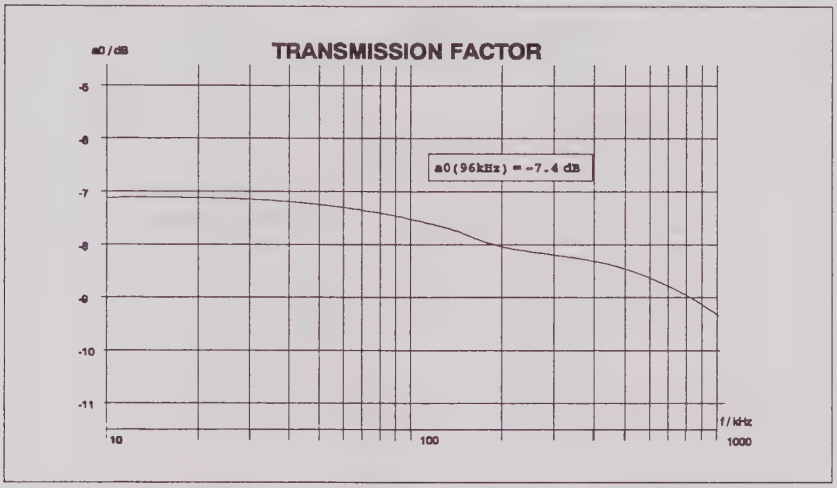


Fig 6 11 Transmission factor a_0

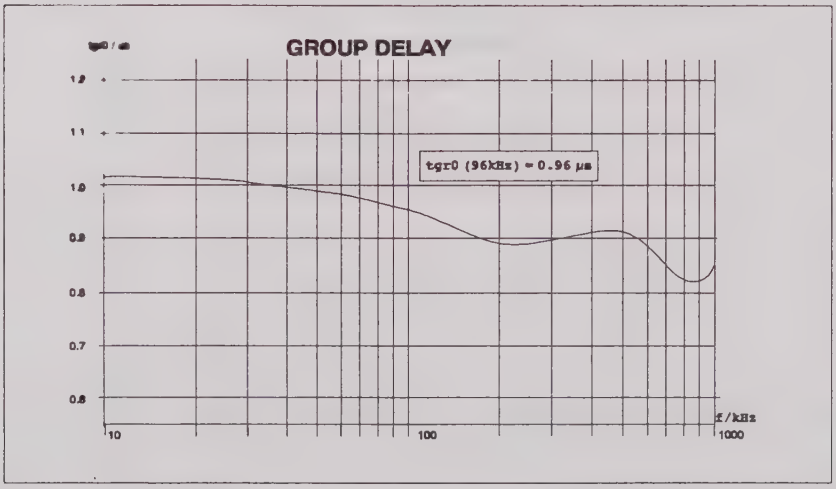


Fig. 6.12: Group delay tgr

The wave impedance Zw is defined using the short-circuit and open-circuit impedance. It can be calculated via a current measurement (voltage at a 50 Ω resistor) and a voltage measurement (U1) (see Fig. 11).

The wave impedance and the phase of the LC Artificial Line for the fundamental wave equal

Zw (96 kHz) = 149Ω ; φ (96kHz) = -14 °

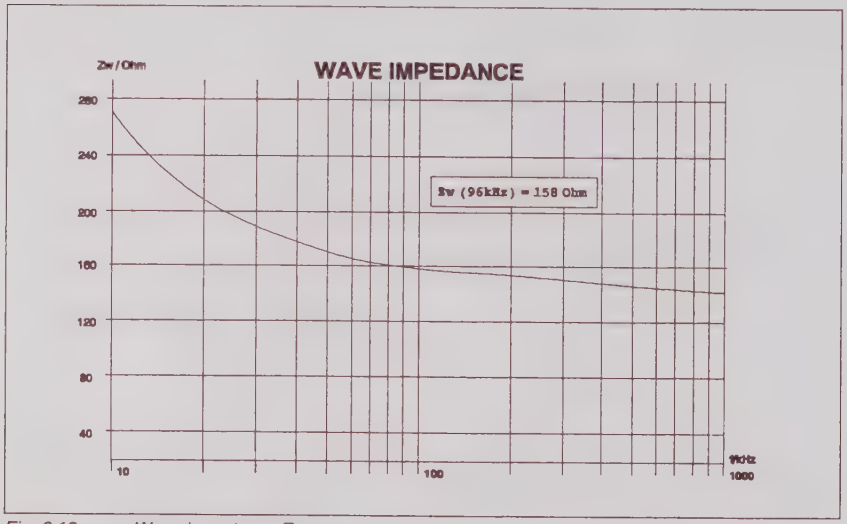


Fig. 6.13: Wave impedance Zw

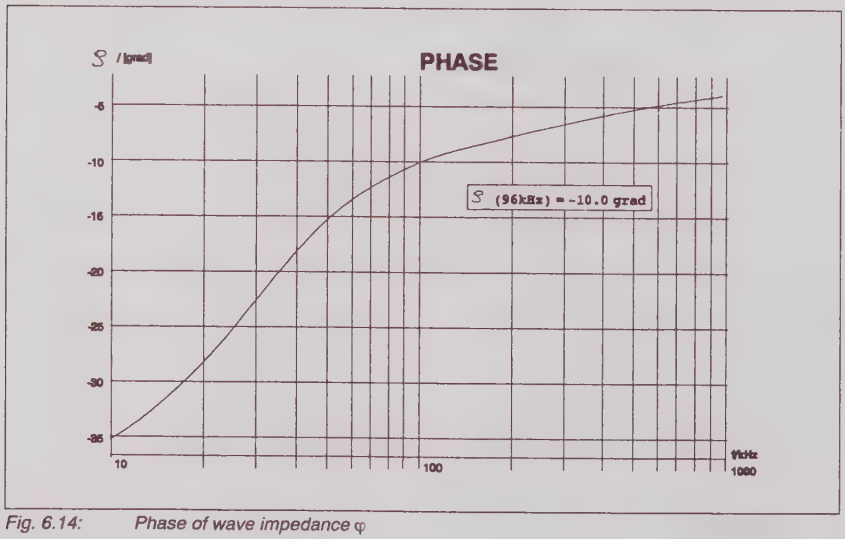
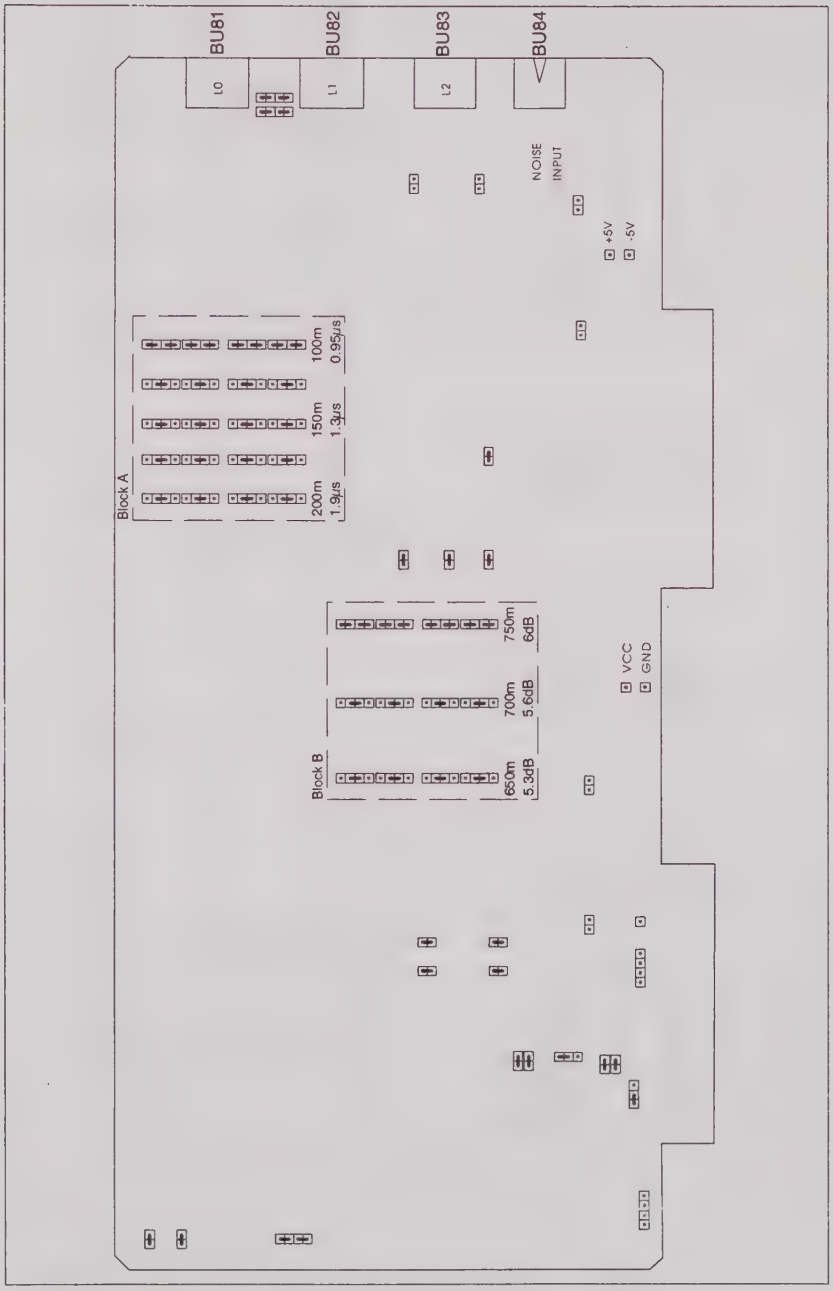


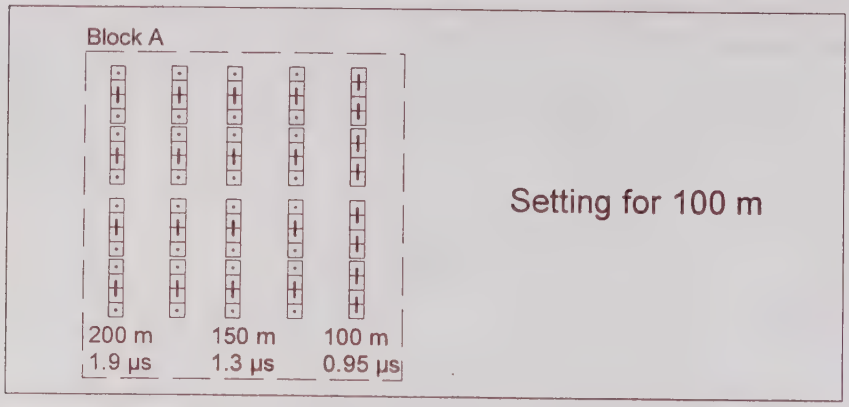
Fig. 6.14: Phase of wave impedance φ

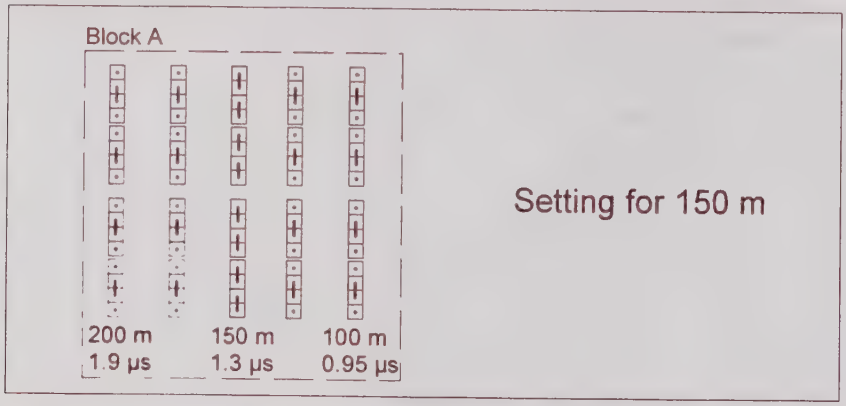
6.3 Position of jumpers and block diagram

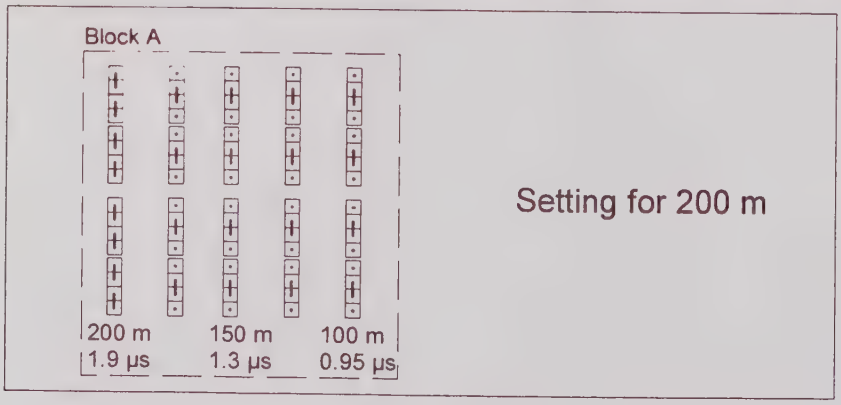
Position of jumpers on PCB

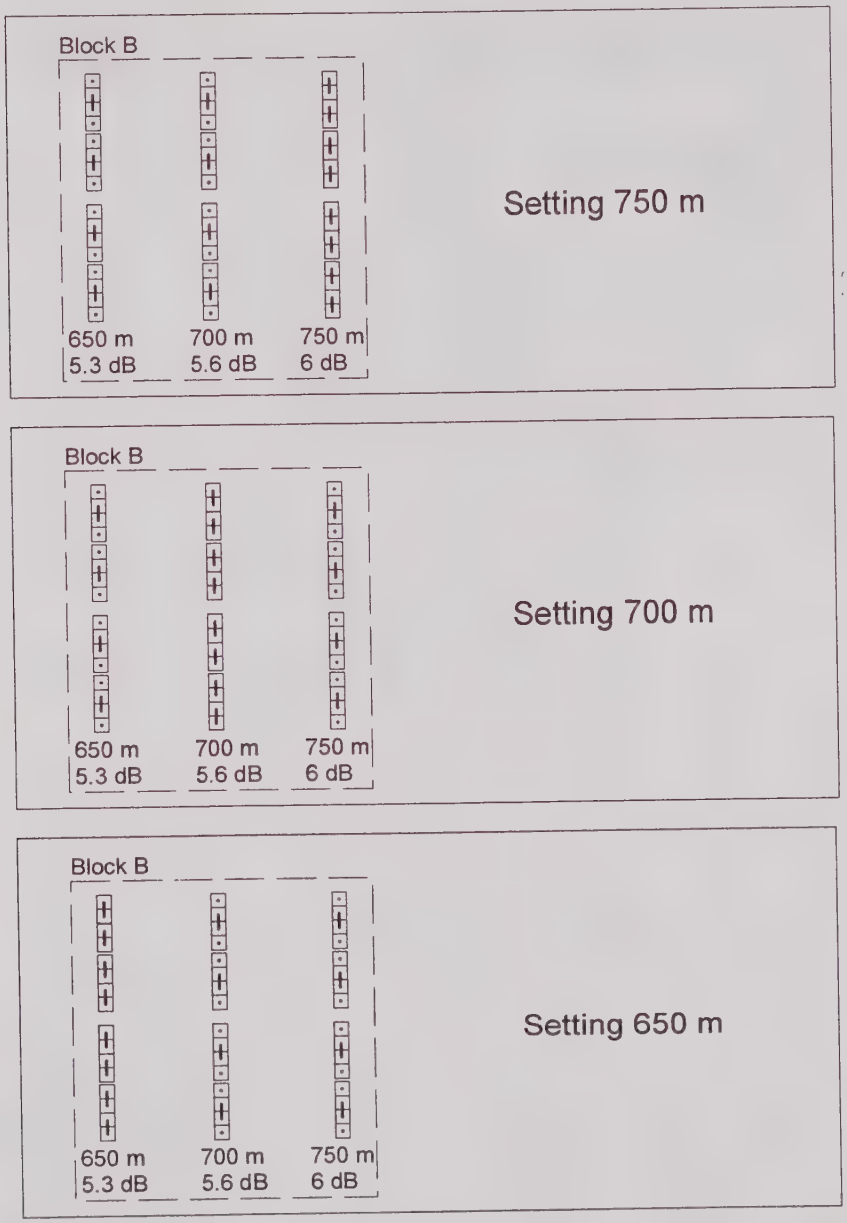


Setting different lenghts via the jumper








Block B
650 m
5.3 dB
700 m
5.6 dB
750 m
6 dB
Setting 750 m
Block B
650 m
5.3 dB
700 m
5.6 dB
750 m
6 dB
Setting 700 m
Block B
650 m
5.3 dB
700 m
5.6 dB
750 m
6 dB
Setting 650 m

Connections of the low-capacitive Artificial Line

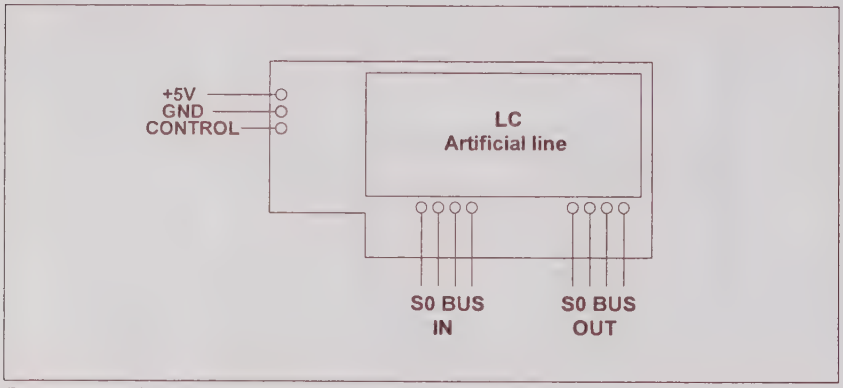
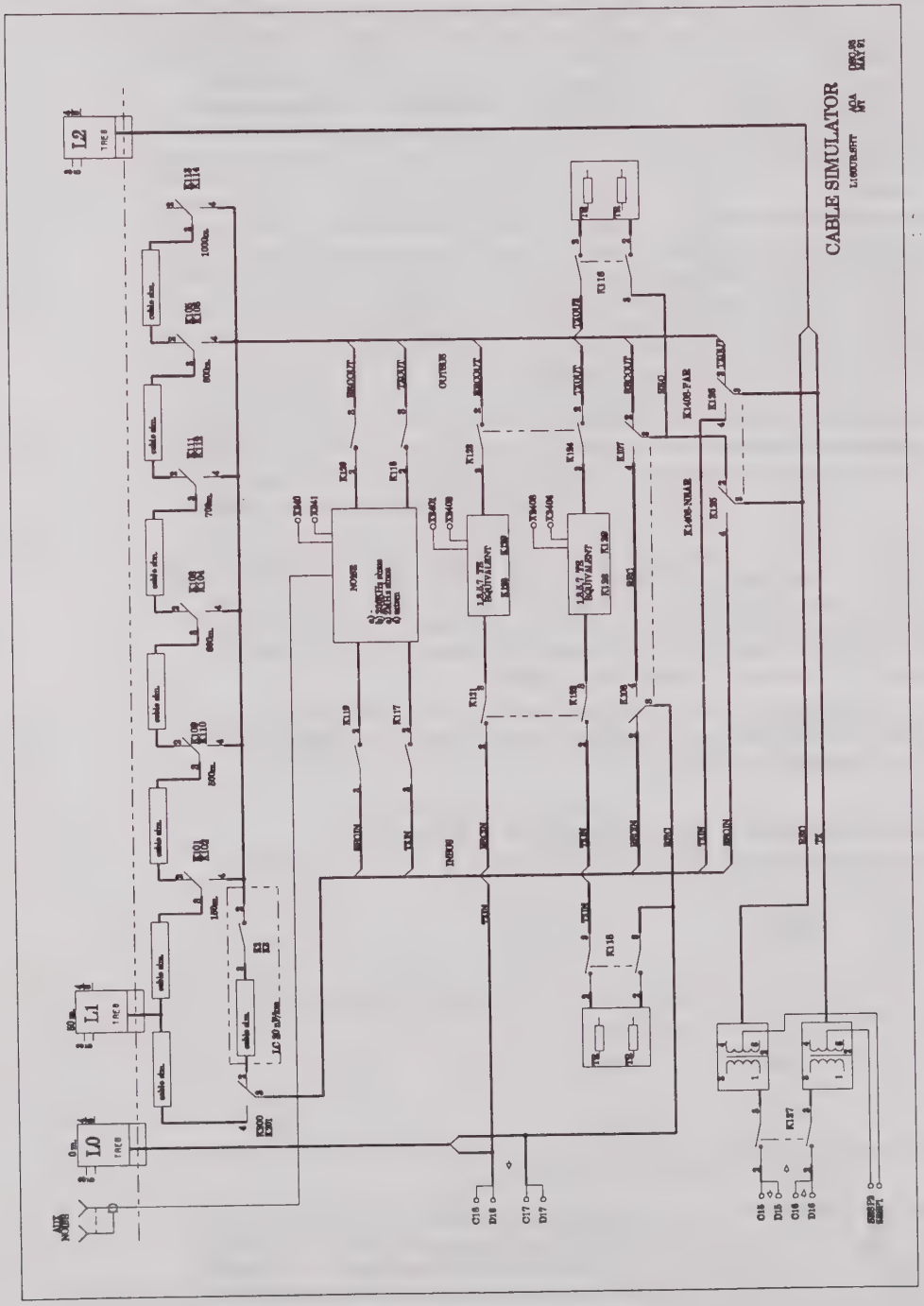


Fig. 6.1: Connections of the module

6.3.1 Block diagram



6.4 Artificial line at base terminal

By means of a switch, which has been slightly modified in comparison to the simple line equivalent circuit diagram, the four-pole response of balanced pair cables to high frequencies can be accurately simulated. The consequences of the skin effect and the sheath loss effect on the cable are taken into account in order to achieve a simulation which is as close to reality as possible. This is successfully accomplished even in cases of high integration levels.

Application of an Artificial Line

Measurements at cable drums or Artificial Lines for balanced pair cables are necessary in order to test the functionality of terminal units (telephones, fax, etc.) and of mains terminal units relative to the medium of transmission. Besides minimal space requirements, the Artificial Lines offer the advantage of making comparative measurements possible, since the influence of manufacturing tolerances common with communications cables no longer applies.

The development of the compact ISDN S_0 Analyzer K1403 of Siemens, which makes all necessary measurements on the S_0 bus possible, raised the question whether a very exact passive simulation of a cable using a minimum of space is feasible. The Artificial Line is intended as a plug-in unit for the K1403 and is limited to one module of 33,5 cm length and 13 cm width. By using it in the K1403, measurements of receiver sensitivity, bit fault rates, jitter and phase relations of the ISDN units in various bus configurations can be performed. This combination is of interest to the user since it saves connecting cables and even an additional unit. Measuring errors due to faulty operation and long connecting lines are reduced, since the object to be tested is connected only to the measuring unit, while all other connections are made automatically inside the latter.

Due to the additional integration of possible connections required according to ITU-T-rec.I430 such as TE loads and interferences, fully automatic measurements at the S_0 bus have become possible with the K1403.

Measuring configurations and requirements of the S_0 bus

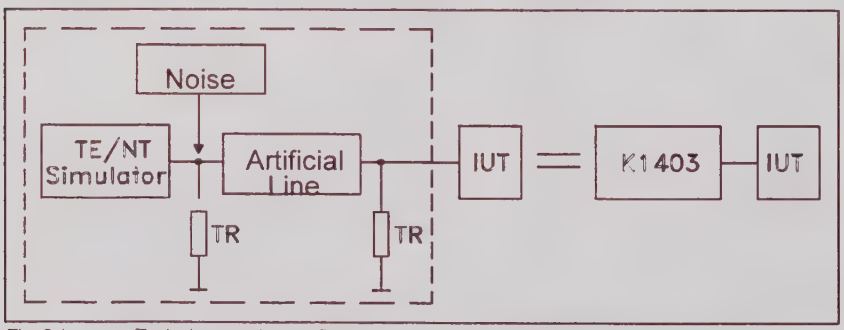


Fig. 6.1: Typical measuring configuration at the ISDN S_0 bus

For each transmission unit at the S0 interface two pair wires are utilized which also serve as feeders. The digital data transmission and the synchronization required by it must be carried out via the S0 bus. Ensuring these functions results in limitations for the lengths of the lines which are defined via attenuation and delay. According to the recommendations of the CCITT /1/ especially two borderline cases in the area of layer 1 in the ISDN need to be checked. Regarding the Artificial Line, this is for

example the response of terminal units at a line with 6 dB attenuation (≈ 750 m) or 1 µs delay (≈ 100 m) at 96 kHz. Because of the high attenuation, a maximum line length of 1 km is prescribed for the necessary measurements in the "worst case" (ITU-T-rec.I430).

Fig. 6.1 shows a simple configuration. This is the point to point connection with a TE/NT simulator at the beginning and an IUT (= ITEM UNDER TEST) as the object to be tested at the end of the line. In order to test the influence of cable-dependent changes in signal shape on receiver response, the Artificial Line must simulate the real characteristics of a cable within a wide frequency range. The main spectral components (the amplitude of the 10th harmonic at appr. 1 MHz is more than 20 dB below the fundamental wave amplitude) of a typical S0 transmission signal reach up to 1 MHz. Thus a bandwidth from DC up to 1 MHz for the Artificial Line is useful to enable simultaneous transmission of supply currents (DC) and digital signals. However, not only attenuation and delay, but also reflexions and transformation characteristics of the cable can influence signal transmission. Especially because of the highly frequency-dependent wave impedance, reflexions at the purely ohmic terminating resistors affect the signal shape /4/. Only a passive simulator for balanced pair cables can fulfill all requirements by simulating the quantities responsible for cable response. The basis for this development is the transmission-line theory with the exact mathematical description of all parameters with which an accurate statement about cable response can be made.

Frequency-dependent permit length (current displacement)

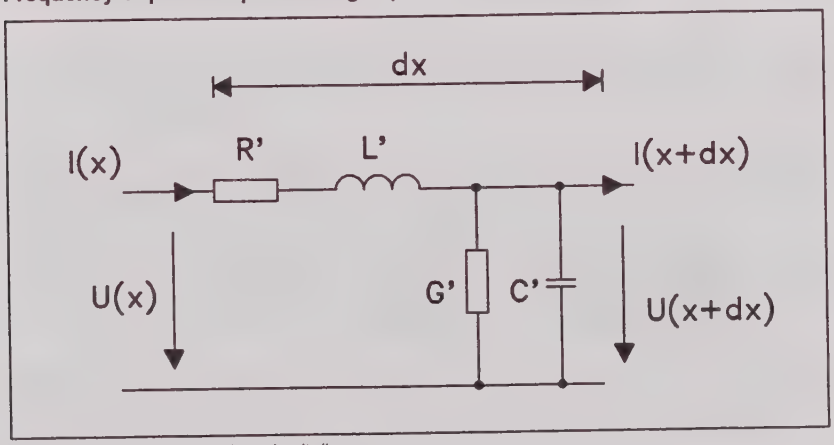


Fig. 6.2: Line equivalent circuit diagram

In the transmission-line theory, the line is modelled in infinitesimal parts for which the quantities per unit length are given. The four-pole response of a cable is completely defined by these quantities. They give the distribution for each kilometer line length and include:

- Capacitance per unit length C' [nF/km]
- Inductance per unit length L' [μH/km]
- Conductance per unit length G' [S/km]
- Resistance per unit length R' [Ω/km]

The conductance per unit length is defined by the loss factor of insulation, the dielectric.

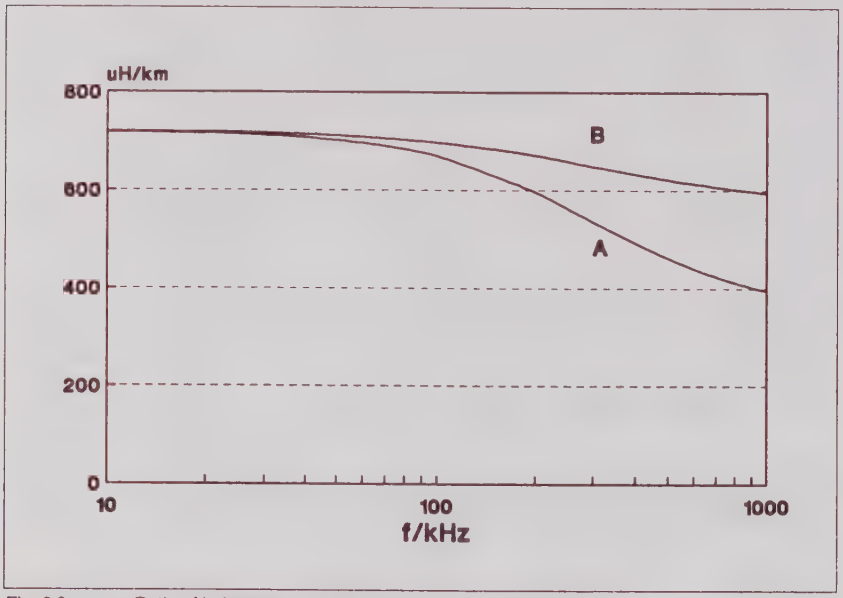


Fig. 6.3: *Ratio of inductance per unit length to frequency*
A: with sheath loss effect
B: without sheath loss effect

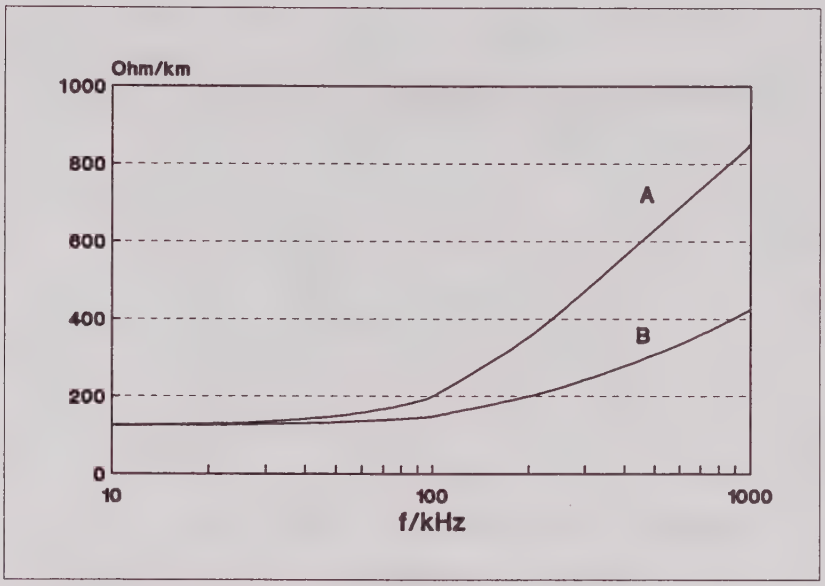


Fig. 6.4: *Ratio of resistance per unit length to frequency*
A: with sheath loss effect
B: without sheath loss effect

Most of the time it can be disregarded in comparison to the capacitance per unit length - more accurately $1/\omega C'$ ($\omega = 2*\pi*f$: angular frequency). The capacitance per unit length is only slightly dependent on the frequency and can be assumed as a constant in first approximation.

The frequency response is defined by the LC behavior of the line as well as by the frequency dependency of resistance and inductance per unit length. Both quantities are affected by the current displacement (skin effect) in the conductor and the sheath. The curve resulting from the ratio between the resistance and inductance per unit length and the frequency for a 0.6 mm copper line with and without metal sheath is shown in Figs 6.3 and 6.4. These curves were calculated taking into account all short-range effects in the cable according to KADEN /2/.

It is easy to see that the effect of the metal sheath in the required frequency range cannot be disregarded, since the attenuation for eaxmple is directly proportional to R'. At 500 kHz, the metal shield increases the resistance per unit length alone by 300 Ω/km.

Producing the skin effect

Resistance and inductance per unit length can be simulated by a passive RL switch - in Fig. 6.6 and Fig. 6.7 Z1 to Z5 (Z1' to Z5') - and a simple line module is obtained.

As it is, the two-stage setup with resistors and inductances can simulate the quantities per unit length of different cables with an accuracy of at least ± 5 % (frequency range from DC to 1 MHz).

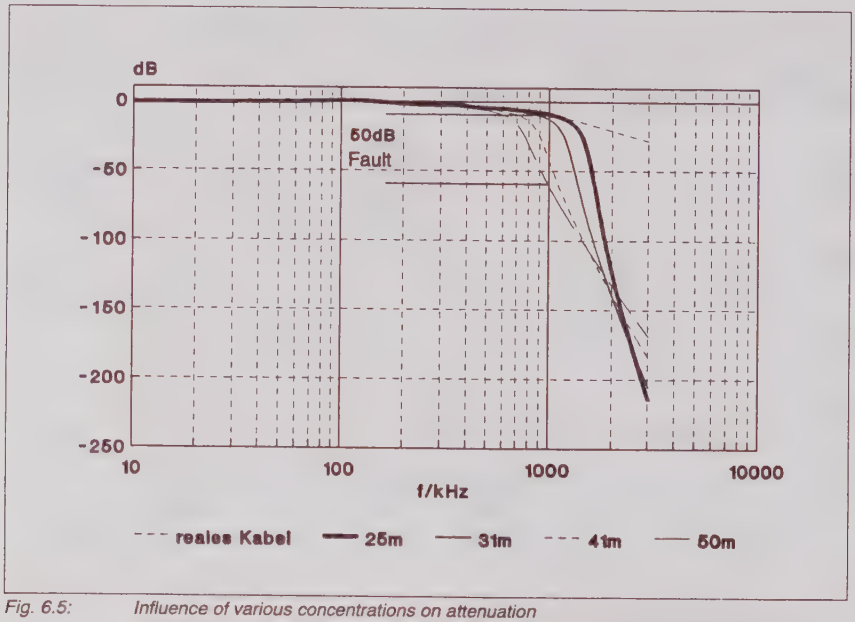


Fig. 6.5: *Influence of various concentrations on attenuation*
Influence of various concentrations on attenuation of a 250 m cable simulated with a series connection of 25 m, 31 m, 41 m and 50 m modules (computer simulation PSpice).

Special problems are now created only by the concentration of the simulator, i.e. the largest reproducible length per simulated unit, since the switch shown in Figs 6.6 and 6.7 simulates a line only for frequencies far below the poles formed by discrete coils and capacitors. In contrast to the cable, the parameters are concentrated and not evenly distributed (the line is not a minimum phase system). Thus, a module with a simulated length of 50 m produces attenuation faults of 50 dB already at 1 MHz for a total length of 250 m. Unlike the line, the switch behaves like a low pass of higher order. The maximum operating frequency is defined by the position of the pole.

This, for example, is the case for

- R' = R0 = 0
- L' = L0 = 700 μH equals 35 μH for each module of 50 m length
- C' = C0 = 120 nF equals 6 nF for each module of 50 m length

one pole with

$\omega p = \sqrt{[1/(LC)]} = 490$ kHz

for one module of 50 m simulated length.

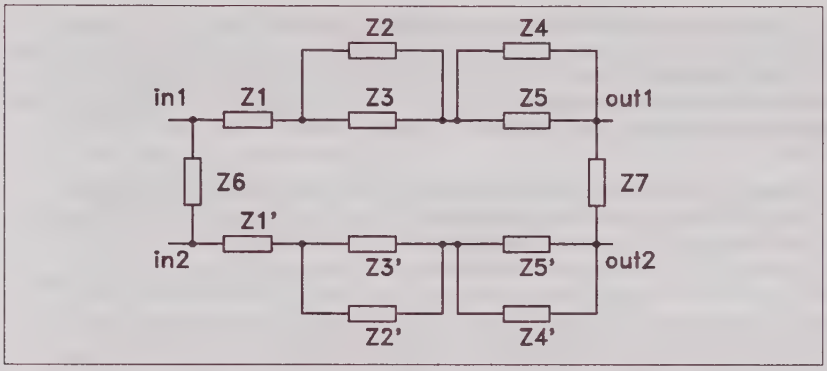


Fig. 6.6: Line module analog to the PI equivalent circuit diagram of the line

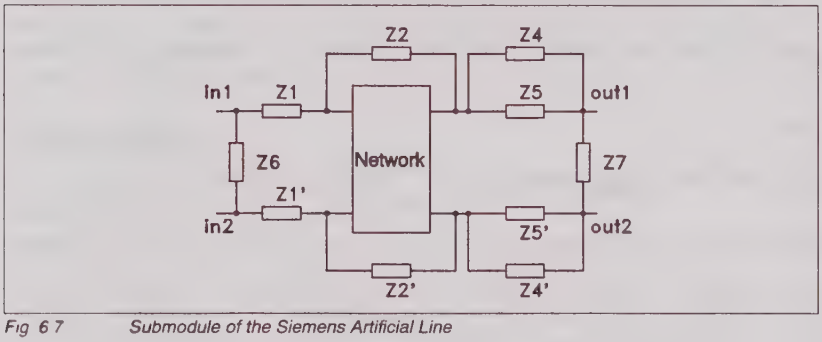


Fig 6 7 Submodule of the Siemens Artificial Line

The high concentration which is necessary because of space limitations leads to faults in the transmission response at higher frequencies /3/. The pole at ωp already produces effects at frequencies lower than ωp. A line of 25 m length which according to Fig 6.5 is apparently short enough shows considerable faults on another scale (Fig. 6.7). This was the starting point for further developments of the switch which should show the least possible deviation from the actual line response at a given concentration up to high frequencies.

6.5 Improvements on the Siemens Artificial Line

The faults in attenuation and delay of a switch according to Fig. 6.6 can be reduced by shortening the simulated length. The question is, however, whether an improvement can be achieved with the same simulated length and all the circuitry required for it.

This was achieved with the Siemens Artificial Line by increasing the distribution of capacities while maintaining the same number of coils. The high packing density required made the use of closed coils necessary anyway in order to avoid parasitic inductive coupling. The symmetrical inductances can be integrated on a core, whereby the connection of further impedances is possible via an additional tap. The switch is thus expanded by a passive network (Fig. 6.7). The success of this principle is demonstrated clearly in Fig. 6.1 in the characteristic of attenuation and group delay.

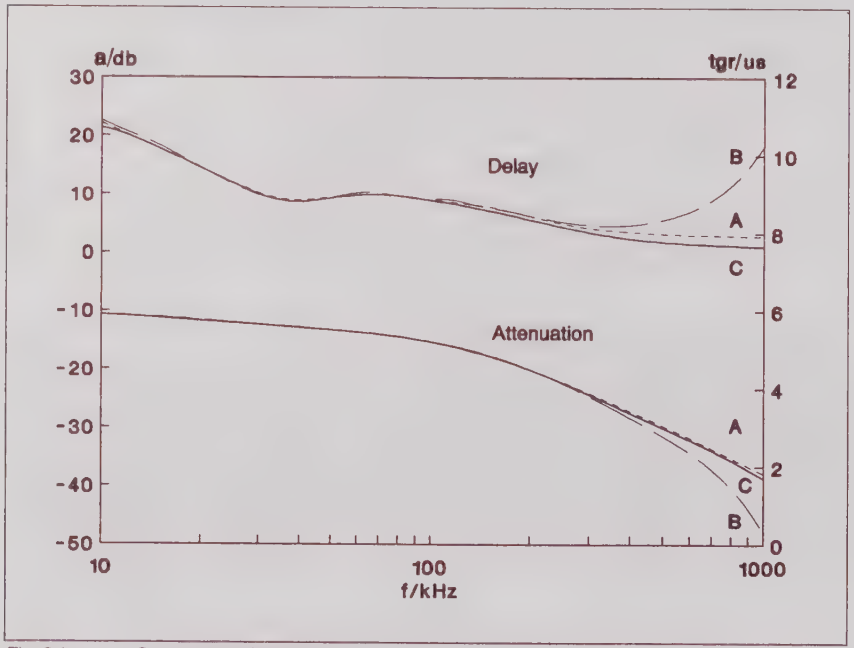


Fig. 6.1: *Comparison of delay and attenuation of both switch types for 1 km cable composed of 25 m modules*
A: Ideal characteristic
B: Switch Fig. 14
C: Switch Fig. 15

The deviation of the attenuation characteristic from the ideal could be reduced from +8 dB/km to +2 dB/km (1 MHz). The group delay shows a deviation of only -300 ns/km instead of +2 µs/km at the start according to Fig. 6.5.

An additional advantage is the low mutual coupling between the line modules, since only closed RM core coils are used. The possible dispersion is also drastically reduced, because the RM core coils can be utilized with a tolerance of 0,1 % to 1 %. Wired coils are not available under 5 %. Besides, saturation via phantom powering is avoided by optimum use of the cores. There is also no saturation with copper cables, since only air inductances occur.

The Artificial Line now responds like a real cable with the respective quantities per unit length regarding attenuation, group delay and wave impedance.

6.6 Final comments

The four-pole response of a cable can now be simulated even in the smallest space with the new switch principle for balanced communications cables. A high reproducibility of cable measurements is now possible, since dispersion could be minimized. The reflexions important for the transmission of digital signals as well as attenuation and delay are simulated with high accuracy. The faults in transmission response of the Artificial Line could be considerably reduced compared to switches commonly used up to now.

6.7 Bibliography

/1/ CCITT I430 blue book, Vol.III Fasc. III 8, Recommendations I310-I470 (I430), Geneva 1989

/2/ Kaden: Wirbelströme und Schirmung in der Nachrichtentechnik, Springer Verlag

/3/ Everett, W.W.: Lumped Model of Transmission Lines - Effekt of Load Impedances on Accuracy, IEEE 1983 Pages 441 to 445

/4/ R. Kallen: Leitungen verändern Impulse, Elektroniker Nr.4-1991 Pages 61 to 65

SIEMENS

ISDN S_0 Analyzer K1403

Electrical Characteristics

User Manual C73000-B6076-C66-1

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CE

The product described in this manual complies with the statutory regulations on electromagnetic compatibility of devices (EMC) or the regulations of the guideline of the council from 03.05.1989 for adaptation of the statutory regulations of the member countries on electromagnetic compatibility of devices (89/336/EEC).

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1 Safety information

The ISDN S_0 Analyzer K1403 has been constructed and tested in accordance with Publication EN61010 Safety Provisions for Electronic Measuring Equipment, and has left the factory in a perfectly safe condition. In order to maintain optimum safety and ensure hazard-free operation, please adhere to the following basic rules.

- Transport the device only in its original packing or by using the transport case specially recommended for the K1403. This will protect the device against shocks.
- The K1403 is exclusively intended for indoor use. Condensation may occur when the unit is brought to its site of operation from a cold environment. Operation is only permissible with an absolutely dry unit after its temperature has adjusted to the environment.
- Before implementing and operating the K1403, make sure that the environmental conditions are complied with. The environmental conditions are listed under the heading "Technical data" in the appendix.
- Before switching on the device, make sure that the preset operating voltage of the device corresponds to the permissible line voltage.
- Make sure that replacement fuses are of the specified type and rating: Use 3.15A/250 V (type T) fuses.
- The power plug must only be inserted into a grounded socket. Do not cancel the protective effect by using an extension cable without a protective ground conductor.
- Make sure that the ventilation slots on the rear and top of the device are not covered.
- The unit can become dangerous if the protective ground conductor is interrupted either inside or outside the unit. Do not interrupt the protective ground conductor intentionally. The same applies when loosening the connection for the protective ground conductor. When opening covers or removing parts, remember that live parts may be exposed if the unit is connected. Connection points may also be live. Disconnect the unit from all voltage sources prior to adjustment, maintenance , repair or when replacing parts. If such work on live and open units cannot be avoided, it should only be performed by qualified staff familiar with the hazard involved.

- All modules contain electro-sensitive components. Please note the necessary precautions and ESD safety measures :

Warning!

When electrical devices are in operation certain parts of these device are live. Non-observance of the above precautions may therefore lead to severe physical injuries or to serious material damage.

Only qualified staff may handle this device or work in its vicinity. They must be thoroughly familiar with all the warnings, safety and maintenance information contained in these instructions. Faultless and safe operation of the device presupposes proper transport, proper storage, set-up and mounting as well as careful handling and servicing.

2 Device description

2.1 ANALOG1

The module ANALOG1 C73249-A11-L8/L80 together with the measuring panel C73249-A11-L11 in the ISDN S_0 Analyzer K1403 enables the measurement of the frequency-dependent longitudinal unbalance and the frequency-dependent impedance at the S_0 interface of ISDN terminal units and network terminators as defined in CCITT I.430. The measurements are carried out according to ETS 300, 012 and CTS-2.

Design and mode of operation

The plug-in module contains three function blocks. The first function block contains a selective level meter for a frequency range from 2 kHz to 1 MHz. The second function block contains a tracking signal generator (level source) for an output frequency of 2 kHz to 1 MHz. The third function block contains a single-loop synthesizer and the frequency conditioner for conversion of the frequency in the receiver and transmitter. The function blocks are controlled by a computer on the module which also handles data transfer and the processing of measured values.

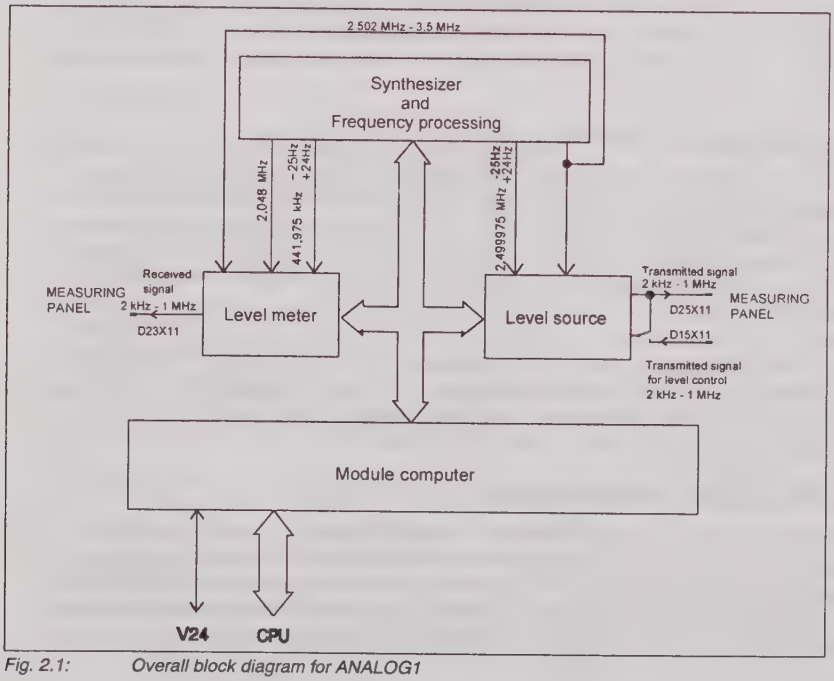


Fig. 2.1: Overall block diagram for ANALOG1

Function description of level meter

The level meter operates according to the heterodyne principle. The signal from the measuring panel is matched in a preamplifier with multi-stage 6-dB level dividers to the input of the first mixer and boosted in this to a frequency of 2.5 MHz. The signal is mixed down to 10 kHz by means of two further conversions and limited in this frequency range to a bandwidth of 25 Hz by a mechanical bandpass. The signal is then amplified, rectified linearly into a quasi-rms value and then evaluated by a 12-bit A/D converter. The result from the setting of the level divider and the evaluation by the A/D converter is processed in the module computer according to the application and transferred together with the frequency information to the main computer for output on the display.

Function description of level transmitter

The level transmitter operates as a beat-frequency transmitter with a signal frequency of 2.5 MHz and a mixed frequency of 2.5 to 3.5 MHz and serves as the signal source for the impedance and longitudinal balance measurements. Its output frequency of 2 kHz to 1 MHz is amplified and applied to the measuring panel as the signal source for the impedance and longitudinal balance measurements. To regulate the amplitude, the transmitted signal is rectified linearly either directly (longitudinal balance measurement) or via the measuring panel (impedance measurement) and applied via a comparator to the control transistor in the 2.5-MHz signal path. The transmitted level is set on the comparator by a D/A converter according to a setpoint/actual-value comparison to the level corresponding to the application.

Function description of synthesizer and frequency processing

The 2-kHz reference frequency of the synthesizer is derived from a temperature-compensated 5-MHz crystal oscillator and boosted in a PLL to a frequency of 100 MHz to 140 MHz. The boosted frequency of the single-loop synthesizer is divided in the transmitter and receiver mixer to 2.5 MHz to 3.5 MHz for frequency conversion. A 50-Hz division is derived from the 2-kHz division in the upper frequency range (100 MHz to 140 MHz) and applied to the converters. The fine resolution of 1 Hz is achieved by pulling a temperature-compensated 5-MHz crystal oscillator. The pulling is monitored by a frequency counter. The signal frequency of the transmitter and the third conversion frequency of the receiver are derived from this oscillator by frequency division and mixing. A further crystal oscillator is used as the basis for the mixing frequency of the second mixer.

Function description of module computer

The module computer controls the three function blocks, evaluates the results, processes these, and delivers the result to the main computer via a FIFO interface. The main computer transfers the information required for the respective application to the module computer via the same interface. In addition to the interface to the main computer, the module computer has another V.24 interface for test purposes.

2.2 ANALOG2

The test module ANALOG2 consists of the following components (cf. block diagram):

- Input amplifier
- Output drive
- AMI decoder
- 75Ω- line driver
- ISDN- S_0 info transceiver
- PRBS generator
- A/D converter
- Sample-and-hold amplifier
- Gate circuit
- Counter
- Pre-trigger and post-trigger
- Clock generator
- Slave CPU
- FIFO interface

The module is used for the following measuring modes:

- Transmitted signal pulse shape on TE and NT
- Frame delay on TE
- Jitter (digital) on TE and NT
- Transmitted signal pulse balance on TE and NT
- Clock accuracy on TE
- Peak current on TE and NT
- Transmitter internal impedance on TE and NT.

The module is also used as the S_0 interface for jitter measurements with the jitter option.

- **Input amplifier**

  The input amplifier is designed as a symmetrical C-coupled broad band amplifier. It is characterized by the high input impedance of approx. 16 kΩ and a CMR of approx. 75 dB at 96 kHz. The module computer sets the gain in a range from approx. 2 dB to 31.5 dB depending on the measuring mode and selected parameters. The gain accuracy is ± 0.05 dB at 96 kHz. The bandwidth is between 30 MHz and 50 MHz depending on the set gain.

- **Output driver**

  The driver converts the internal NRZ signals to AMI code and adjusts an output amplitude of 750 mV. The output lines are connected via capacitors to the internal measuring panel and can be disconnected via a relay depending on the operating status of the module.

- **AMI decoder**

  The AMI decoder generates two NRZ signals from the amplified S_0 received signal. These two signals are applied to the info transceiver and the counter gate circuit.

- **75Ω- line driver**

  This line driver is used to decouple the amplified received signal. This signal can be applied from the rear BNC socket e.g. to an external oscilloscope. The amplitude of the input signal can be determined using the three gain values in the case of a 75-Ω terminator.

Internal impedance	R_i = 75Ω
Bandwidth	BW ≈ 30MHz
Tolerance	Δv = ± 0.25 dB at 96 kHz with 75Ω terminator (± 0.1 % resistance)

Type of measurement	Gain
Pulse shape; 5.6Ω	21,46 dB
Pulse shape; 50Ω	9,87 dB
Pulse shape; 400Ω	1,87 dB
Peak current	31,46 dB

Table 2.1: Level diagram of broadband amplifier (ANALOG2)

- **ISDN S_0 info transceiver / PRBS generator**

  The ISDN S_0 info transceiver is the core of the ANALOG2 module. It can send and detect all information under computer control. Switching between TE and NT modes is carried out depending on the device configuration. The corresponding frame clock signals are generated for the receiver and transmitter frames. The following functions can be set together with the PRBS generator:

	Function in TE mode	Function in NT mode
TRANSMIT	INFO0	INFO0
	INFO1	INFO2
	INFO3 with "1" in the data channels	INFO4 with "1" in the data channels
	INFO3 with "0" in the data channels	INFO4 with "0" in the data channels
	INFO3 with PN in B1+B2+D	INFO4 with PN in B1+B2+D
		INFO4 with '0AAhex' in B1+B2
DETECT	INFO0	INFO0
	INFO2	INFO1
	INFO4 with "1" in the data channels	INFO3 with "1" in the data channels
	INFO4 with '≠1' in the data channels	INFO3 with '≠1' in the data channels

Table 2.2: Transmitter and receiver infos at ANALOG2

Quasi-random sequences with lengths

$$2^9\text{-}1,\ 2^{11}\text{-}1,\ 2^{13}\text{-}1,\ 2^{15}\text{-}1,\ 2^{17}\text{-}1,\ 2^{19}\text{-}1$$

can be set as PRB sequences in the menu, and also the transmitted patterns binary "0", binary "1" and alternating patterns "1"/"0AAhex", each in 40 frames.

- **A/D converter/sample-and-hold amplifier**

  The A/D converter has a resolution of 11 bits plus sign. Its input signal is applied from the sample-and-hold amplifier via an intermediate impedance converter. The sample-and-hold amplifier is designed for a bandwidth of approx. 50 MHz and settling times of approx. 10 ns.

- **Gate circuit**

  The gate circuit is configured by the module computer for the respective measuring mode. In the case of all types of measurement based on pulse shape measurements (pulse shape, pulse unbalance, peak current and impedance of the active transmitter), the gate circuit generates the control signals which start and stop the counter sequences required for the multi-period sampling procedure (MPS; see description of pulse shape measurement). In the case of the frame delay measurement, the counter sequences are enabled by the F/L bit of the transmitter frame and disabled by the F/L bit of the receiver frame. The gate circuit also detects all negative full edges of the received signal. These edges start the count in the case of jitter measurements; the count is stopped again by the next edge of the 192-kHz reference clock.

- **Counter**

  The counter sequences are configured by the module computer depending on the selected type of measurement:

Type of measurement	Counter configuration	Reference clock
Pulse shape and all derived measuring modes	2 x 8-bit-Synchronzähler	16 MHz (double pulses) 24 MHz (single pulses)
Frame delay	16-bit async. counter	48 MHz
Jitter	8-bit sync. counter	48 Mhz/192 kHz
Clock accuracy	16-bit async. counter	1 s,5 s (48 MHz)

Table 2.3: Counter configuration in relation to measuring mode (ANALOG2)

- **Pre-trigger and post-trigger**

  It is necessary to compensate the cycle delay depending on the test object in the case of these modes based on the pulse shape measurement. The result is that the measured pulse is positioned in the tolerance mask. The actual position of the measured pulse relative to the tolerance mask is thus automatically calculated during the measurement, and the setting of the pre trigger and post trigger circuits are then made. The setting range covers ± ½ UI (1 UI = 5.208 µs = 1/192 kHz). The resolution is approx. 21 ns.

- **Clock generator**

  All clock signals required are generated by the clock generator. These signals are the derivatives of the 48-MHz reference oscillator (± 5 ppm) as well as 12.288 MHz and auxiliary clock signals divided down from this. A 12.28-MHz oscillator is also coupled-in in TE mode; its frequency offset supports recovery of the clock and suppression of jitter on the received INFO4 of the NT.

- **Slave CPU/FIFO interface**

  An 8-bit microcomputer of type 80C452 is used as the module computer. This contains an 80C32 core and a FIFO interface for connection to the main computer. The module computer carries out all settings dependent on the type of measurement, monitors and controls the measuring sequence, records the measured data and executes data processing. Complete results in arithmetic format (IEEE floating-point, single precision) are transmitted to the main computer during the measurement and also following the stop in some cases. Processing of the measured data, i.e. calculation of results based on ETSI 300_012, is carried out by the module computer.

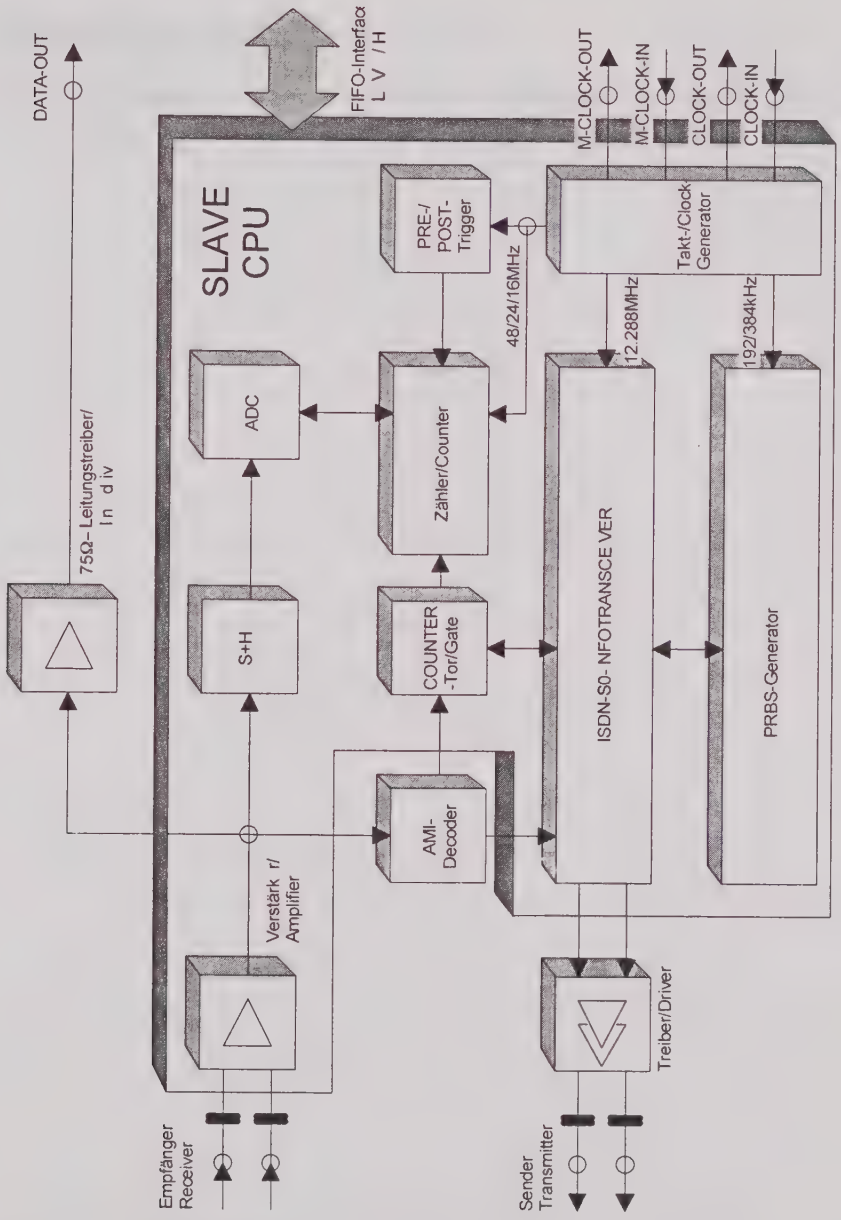


Fig. 2.2: Overview plan ANALOG

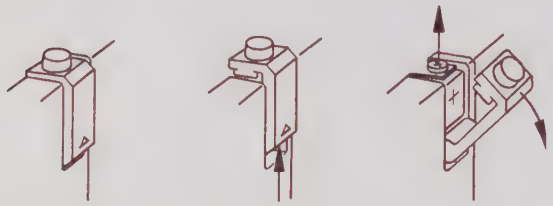
3 Start-up preparations

The following pages will tell you how to make the ISDN S_0 Analyzer ready for use. It will also tell you what you must observe when mounting the K1403 modules.

3.1 Mounting a module

First, remove the cover of the device. The fixing screws for the cover are covered by four corner latches. Proceed as follows:

➤ Push the corner latches some 4 mm upward in direction of the arrow and unhinge the corner latches.



➤ Loosen the four screws which are now accessible and remove the cover.

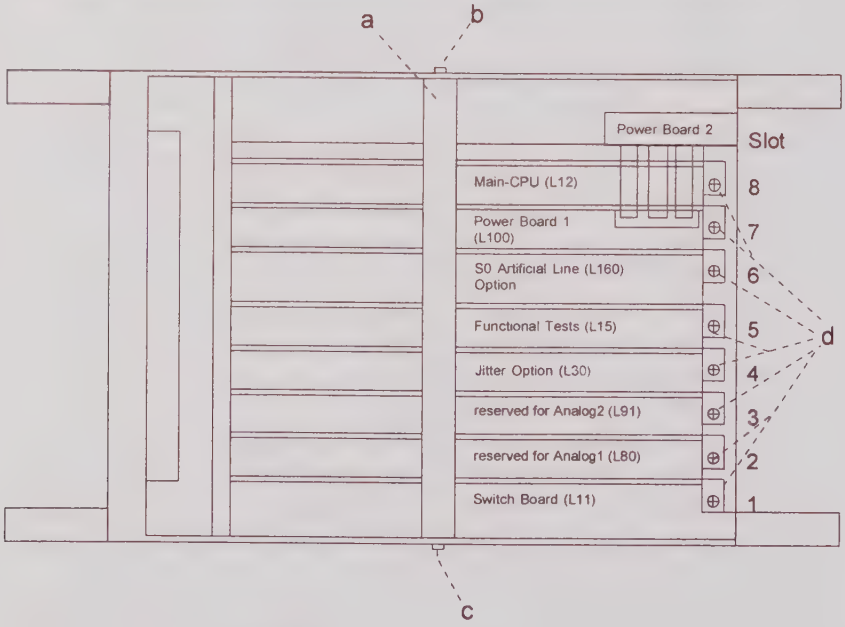


Fig. 3.1: Set-up of the modules

➤ Take the support (a) out by removing screws (b) and (c).

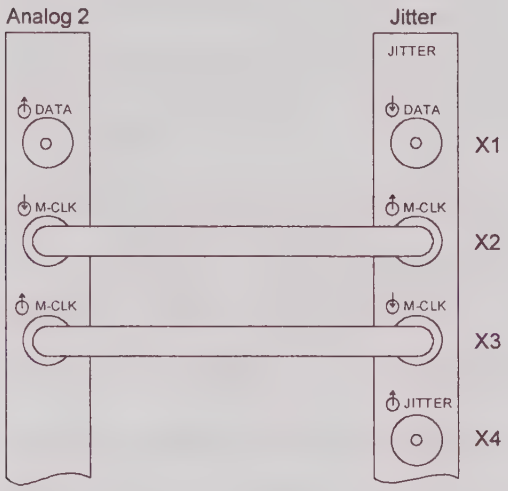
➤ Loosen the module slot screw (d). Insert the module into its destined slot. Ensure that it is correctly assigned and properly fitted in the guide support.

➤ Tighten the module slot screw (d). Re-mount the support (a): Position the printed board in the grooves of the support and tighten screws (b) and (c).

➤ Re-attach the cover of the device.

3.2 Connection of the coaxial cables

For FRAME DELAY measurements, the modules Analog2 and Jitter must be connected with each other as follows:



4 Operation

The required measuring mode, the test parameters and all equipment parameters are clearly arranged on a large, self-luminous electroluminescent display and set with the aid of operator prompting (menu technique).

Operator prompting is performed with selection windows and interactively changing softkey combinations. Functions or parameters are selected by simply touching the relevant part of the touch screen. No pressure needs to be exerted. Each selection is acknowledged by inversion and is implemented when the panel is exited.

If several setting parameters are offered, these are combined into a single selection window. This window appears after the parameter, e.g. transmitted level has been selected and is deleted after a value has been selected.

There are only two menu levels: the basic menu (which appears after switch-on) and the working menu. The latter is actively adapted, i.e. expanded or simplified, to the given setting or operating mode (START, STOP, RESULT).

Only those touch panels which are necessary or expedient for an application are faded in. Other possibilities need not be taken into account.

4.1 Control elements and sockets

ANALOG1/ LEVEL METER input BU41

The input signal of the ANALOG1 module is available during the measuring modes Impedance and Unbalance.

Max. input level U_{emax} = 4,4 Vss (+6 dBm)

Input resistance R_e = 10 kΩ

ANALOG1/ LEVEL METER output BU42

Together with input BU41, transmitter output BU42 is intended for connecting external test set-ups. BU42 supplies a sinusoidal signal which can be set via the menu.

Transmitted signal amplitude U_{rms} = 100 mV ... 1 V

Output resistance Ra ≤ 20 Ω

Where impedance measurements are performed via the measuring panel, the transmitted level varies as a function of the test object and the transmitted frequency since an AGC controller is connected.

ANALOG2 DATA output

The amplified signal of the receive line of the K1403 is available at this socket. This output is provided e.g. for monitoring purposes and subsequent applications.

Output resistance R_i = 75 Ω

Bandwidth BW ≈ 30 MHz

Tolerance Δv = ±0.25dB to 10kHz

Measuring mode	Gain
Pulse shape; 5.6 Ω	21.46 dB
Pulse shape; 50 Ω	9.87 dB
Pulse shape; 400 Ω	1.87 dB
Peak current	31.46 dB

Input signal amplification for various measuring modes (ANALOG2)

ANALOG2 M-CLK input

The clock output of the jitter option, an external jitter generator or the output of a through-modulator is connected to this socket. The test pattern generator (INFO generation) can thus be supplied with a jittered system clock in order to jitter the transmitted signal. Switchover to external clock generation is performed in the menu.

Input center frequency f_{center} = 12.288 MHz

Input level Ue: CMOS (no overvoltage protection; R_e = 200 Ω)

ANALOG2 M-CLK output

The clock input of the jitter option or the input of a through-modulator is connected to this socket. The system clock of the ANALOG2 module can then be used as the reference clock for the jitter generator of the jitter option or for a through-modulator.

Output frequency f_{center} = 12.288 MHz

Output level Ua: CMOS (no short-circuit protection; R_i=10 Ω)

ANALOG2 transmitter clock / CLOCK input

This socket is reserved for subsequent applications.

ANALOG2 transmitter clock / CLOCK output

The output supplies the system clock of the test pattern generator (INFO generation). The signal can be passed on to an external through-modulator for jittering.

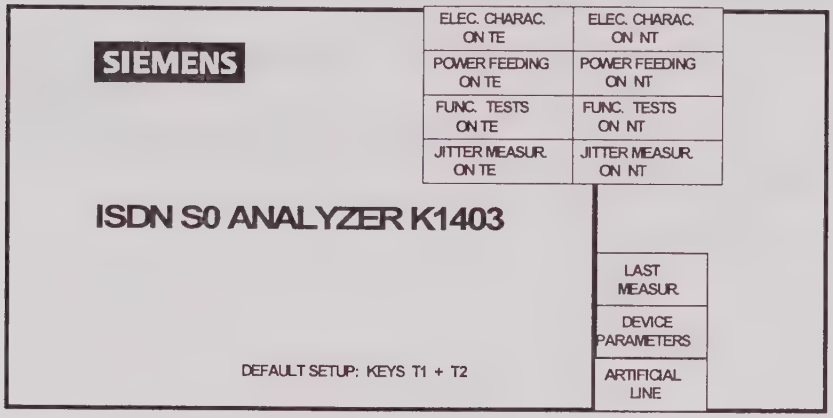
Output frequency f_{sys} = 1.54 MHz

Output level Ua : CMOS (no short-circuit protection!)

This output is reserved for subsequent applications.

The DATA, M-CLK input and M-CLK output sockets must be connected to the corresponding DATA-IN, CLK output and CLK input sockets of the jitter option 7KK1403-2AD if this module is inserted.

4.2 Summary of operation



5 Measurements and presentation of results

5.1 Electrical measurements TE

5.1.1 Impedance

(ETS §A.8.5.1.2 Test A&D; §A.8.6.1.1 Test A&C)

			TRANSMIT LEVEL 200 mV rms	TOL-MASK OFF
			FREQUENCY RANGE 2 KHZ - 1MHZ	
MEASUREMENT (TE) IMPEDANCE	TANS./REC. TRANSMITTER		POWER FEEDING NORMAL 32V	

Setting parameters (MENU)

MEASURE-MENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
OUTPUT PHASE DELAY
CLOCK ACCURACY
IMPEDANCE TRANSMITTER ACTIVE
PULSE UNBALANCE
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY

TRANS./REC.	TRANSMIT LEVEL	TOL. MASK	FREQUENCY RANGE	POWER FEEDING
RECEIVER	EDIT	OFF	EDIT	PASSIVE
TRANS-MITTER	LAST EDIT VALUE	ON	LAST EDIT VALUE	NORMAL
	CCITT	ON WITH CONF. TEST	2 KHZ-1MHZ	RESTRIC-TED
	100 mV rms		2 KHZ-40 KHZ	EXTERNAL
	200 mV rms		10KHZ-200KHZ	
	300 mV rms		50KHZ-1MHZ	
	400 mV rms			
	500 mV rms			

Dependencies

The following dependencies exist in this menu:

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24V	24V	-
-	32V	32V	-
-	42V	42V	-

Measured quantity

The parameter is the frequency-related magnitude of the impedance of the TE receiver or the passive transmitter (transmitted signal "0"). The test object is in the deactivated status (F3).

Test method

A sinusoidal test voltage is applied to the test object. The current in the test circuit is measured for different test frequencies between 2 kHz and 1 MHz. Measurement is performed relative to a reference resistance (200 Ω). All the effects of thermal drift or internal frequency dependencies are minimized through calibration and reference measurements. The calibrating measurement is carried out automatically when the first measurement is activated after switch-on and is repeated cyclically during the measurement.

The reference measurement is currently run before the first measurement and then only if setting parameters have been changed and the measurement restarted or when there is a new start after a calibrating measurement.

Starting from mid 1996 a new board ANALOG1 is in use. With its release version C73249-A11-L80, the reference measurement is run prior to each measurement. Further more no calibration steps for the transmitter and receiver are necessary anymore.

In the case of an external supply, a minimum voltage of 30 V must be applied.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG1 are initialized. The following status message appears in the display

```
INIT/START
```

If the ANALOG1 module is used, transmitter and receiver calibration is then performed automatically for the first measurement performed each time the unit is switched on and at intervals of approx. 10 minutes thereafter. Automatic calibration takes approx. 20 s and is acknowledged by the two status messages

CALIBR.SEND

CALIBR.REC

After each measurement START, a reference measurement is first performed for the relative measurement. This takes approx. 15 s and is indicated by the following message.

REFERENCE

The start of the measurement itself is indicated by

MEASURE

A complete test cycle in the selected frequency range, including all calculations, evaluations and graphic output on the display, requires approximately t_{MESS} ≈ 15 secs.

The START/STOP key must be depressed again to stop the measurement. The following appears

STOP

Presentation of results (RESULT)

The results are presented during the measurement in graphic form (see below). The displayed results are overwritten cyclically each time the frequency range is run through, the current test point being indicated by a continuous bar cursor.

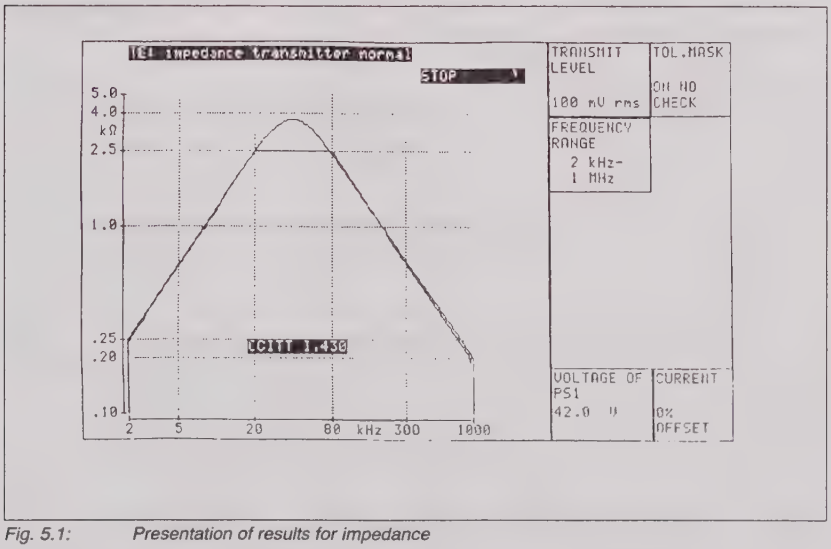


Fig. 5.1: Presentation of results for impedance

The axes are inscribed in accordance with the selected parameters. A double logarithmic inscription and presentation are used.

The RESULT key (T2) can be used to change to a "results mode" after the measurement has been terminated with T3. The results can now be indicated numerically point for point using a superimposed line cursor. The tolerance violations are indicated with a superimposed tolerance curve (marked "NC").

Measured values are displayed in the following form

```
Frequ.: 3.450  kHz      Imped.: 2.244   kΩ
```

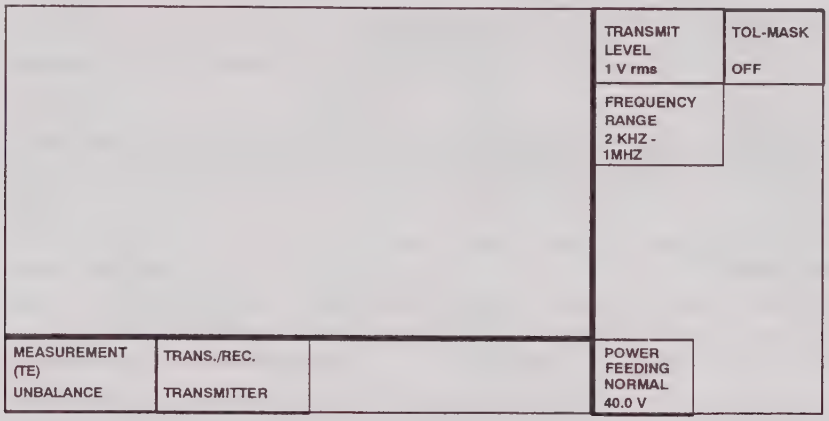
The cursor can be displaced roughly on the x-axis by touching the required frequency range (approx. ± 15 pixels). It is also possible to move them pixel by pixel to the left or right with the two touch fields

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.1.2 Unbalance

(ETS §A.8.5.6.1.; §A.8.6.4)



Setting parameters (MENU)

MEASUREMENT	TRANS./REC.	TRANSMIT LEVEL	TOL. MASK	FREQUENCY RANGE	POWER FEEDING
IMPEDANCE	RECEIVER	EDIT	OFF	EDIT	PASSIVE
UNBALANCE	TRANS-MITTER	LAST EDIT VALUE	ON	LAST EDIT VALUE	NORMAL
PULSE SHAPE		CCITT	ON WITH CONF. TEST	2 KHZ-1MHZ	RESTRIC-TED
FRAME DELAY		1 V rms		80 KHZ-1 MHZ	EXTERNAL
CLOCK ACCURACY		0.9 V rms			
IMPEDANCE OF ACTIVE TRANSMITTER		0,8 V rms			
PULSE UNBALANCE		0,7 V rms			
PEAK CURRENT					
JITTER					
RECEIVER SENSITIVITY					

Dependencies

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24V	24V	-
-	32V	32V	-
-	42V	42V	-

Measured quantity

The frequency-related unbalance against the protective earth (longitudinal conversion loss LCL) is measured at the TE input and TE output in both the following statuses F1: inactive; F3: deactivated.

Test method

A sinusoidal test voltage is applied to the test object. The voltage U_T at the output or input of the test object is measured relative to the test voltage U_P for various test frequencies between 2 kHz and 1 MHz. Measurement is performed relative to a reference unbalance. All effects of thermal drift or internal frequency dependencies are minimized with calibration and reference measurements

$$a_{LCL} = 20 \cdot \log \frac{|U_P|}{|U_T|} \text{ dB}$$

The reference measurement is currently run before the first measurement and then only if setting parameters have been changed and the measurement restarted or when there is a new start after a calibrating measurement.

Starting from mid 1996 a new board ANALOG1 is in use. With its release version C73249-A11-L80, the reference measurement is run prior to each measurement. Further more no calibration steps for the transmitter and receiver are necessary anymore.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG1 are initialized. The following status message appears in the display

```
INIT/START
```

If the ANALOG1 module is used, transmitter and receiver calibration is then performed automatically for the first measurement performed each time the unit is switched on and at intervals of approx. 10 minutes thereafter. Automatic calibration takes approx. 20 s and is acknowledged by the two status messages

```
CALIBR.SEND
```

```
CALIBR.REC
```

After each measurement START, a reference measurement is first performed for the relative measurement. This takes approx. 10 s and is indicated by the following message.

REFERENCE

The start of the measurement itself is indicated by

MEASURE

A complete test cycle in the selected frequency range, including all calculations, evaluations and graphic output on the display, requires approximately t_{MEAS} ≈ 10 secs.

The START/STOP key must be depressed again to stop the measurement. The following appears

STOP

Presentation of results (RESULT)

The results are presented during the measurement in graphic form (see below). The displayed results are overwritten cyclically each time the frequency range is run through, the current test point being indicated by a continuous cursor at the bottom of the screen.

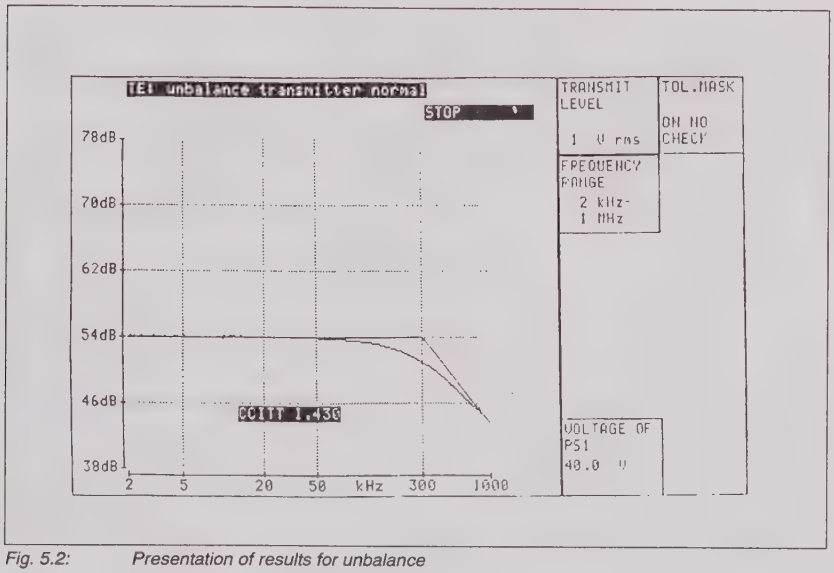


Fig. 5.2: Presentation of results for unbalance

The axes are inscribed in accordance with the selected parameters. A double logarithmic inscription and presentation are used.

The RESULT key (T2) can be used to change to a "results mode" after the measurement has been terminated with T3. The results can now be indicated numerically point for point using a superimposed line cursor. The tolerance violations are indicated with a superimposed tolerance curve (marked "NC").

Measured values are displayed in the following form:

```
Frequ.: 2.095 kHz  Level: 71.23 dB
```

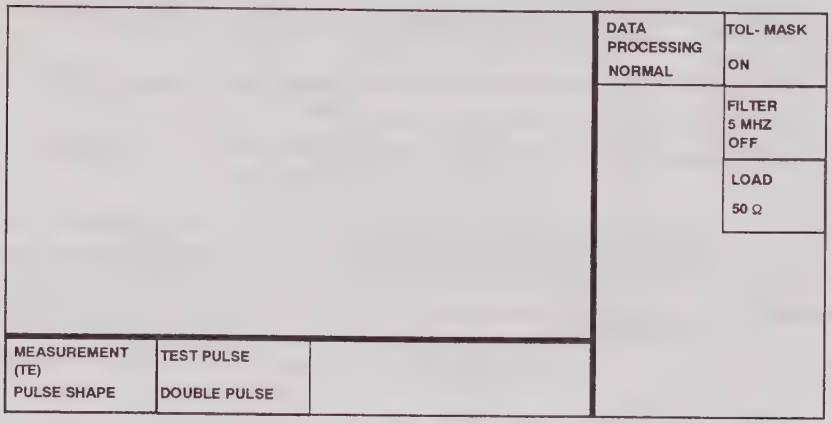
The cursor can be displaced roughly on the x-axis by touching the required frequency range (approx. ± 15 pixels). It is also possible to move pixel by pixel to the left or right with the two touch fields

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.1.3 Pulse shape

(ETS §A.8.5.3; §A.8.5.5.1; §A.8.5.5.2)



Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
FRAME DELAY
CLOCK ACCURACY
IMPEDANCE OF ACTIVE TRANSMITTER
PULSE UNBALANCE
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY

TEST PULSE	DATA PROCESSING	TOL. MASK	FILTER 5 MHZ	LOAD	POWER FEEDING
POSITIVE	NORMAL	OFF	OFF	5.6 Ω	PASSIVE
NEGATIVE	MAX. VALUES	ON	ON	50 Ω	NORMAL
DOUBLE PULSE	MIN. VALUES			400 Ω	RESTRICTED
	MEAN VALUE				EXTERNAL

Depencencies

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24V	24V	-
-	32V	32V	-
-	42V	42V	-

TOL. MASK	
OFF	ON
-	DATA PROCESSING
(NORMAL)	NORMAL
-	MAX. VALUES
-	MIN. VALUES
-	MEAN VALUE

Measured quantity

When measuring pulse shape, the shape of the TE transmitter signal is recorded. It is possible here to record either an individual positive or negative pulse or a double pulse (F/L bit).

Test method

The terminal equipment TE is brought to the active status (F7) by means of INFO4 and transmits INFO3. A test pattern can be transmitted in the B-channels and D-channel in order to generate individual pulses. A data loop or a special test mode is required for this purpose in the test object TE. A trigger window is activated by masking the required pulse (hardware). A total of 256 test points are recorded in this trigger window (MPS method, multi-periodic sampling). If single pulses have been selected for measurement, the software automatically searches for an isolated single pulse in the receiver frame during the measurement. The trigger mask is shifted until the trigger condition (low, high, low level) is satisfied. The following message is output in the display during the search and if a single pulse cannot be found:

```
AN2: NO TRIGGER
```

The following can be selected for data processing

- Normal — Unmodified display of pulse shape
- Maximum value — Only display of largest amplitude values per position on the x-axis
- Minimum value — Only display of the smallest amplitude values per position on the x-axis
- Mean value — Only display of exponential mean value of all measured values per position on the x-axis

The hold function for minimum or maximum values can also store peaks which are non-recurring and also infrequent to enable the examination for tolerance violations. The mean function enables increasingly precise determination of the measured value per position on the axis as the measuring period proceeds. The exponential mean value simulates the function of a 1st order low-pass filter. The exponential mean value is calculated according to the following equation

$$M_n = M_{n-1} + \frac{P_n - M_{n-1}}{K}$$

where: M_n = current mean value; $n \in N_0$
P_n = current measured value
K = averaging constant; K=32

The advantage of this method is that a filter can be implemented without bandwidth losses. The calculation time required slows down the measuring cycle, however. The effects of the three types of data processing are shown below. The first figure shows the max. and min. values for a double pulse on a 400-Ω load.

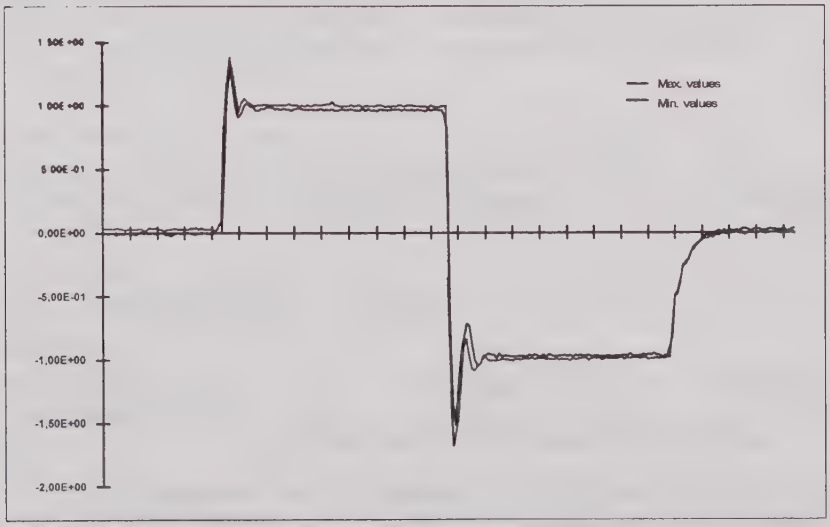


Fig. 5.3: Double pulse at 400Ω (display of maximum/minimum value)

The following figure shows the effect of exponential mean-value generation using the example of a single pulse on a 5.6-Ω load. The normal voltage response is shown at the top, and the averaged response at the bottom.

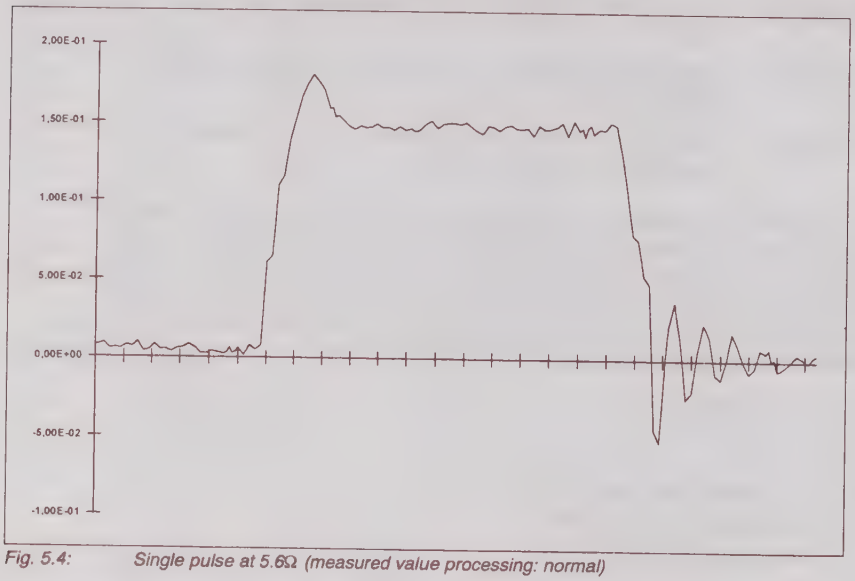


Fig. 5.4: Single pulse at 5.6Ω (measured value processing: normal)

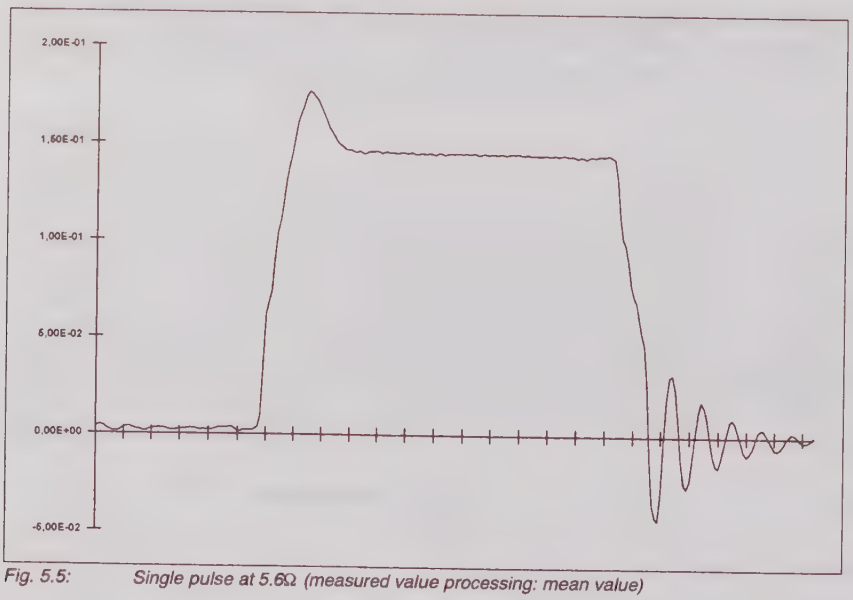


Fig. 5.5: Single pulse at 5.6Ω (measured value processing: mean value)

A reduction in the noise level can also be achieved at the same speed but with a reduced bandwidth (5 MHz) using the selectable 3rd order low-pass filter. The accuracy of the amplitude. however, is reduced to ± 2 % of the measured value ±15 mV.

The different effects of the two filters can be recognized below by superimposing an averaged single pulse and one measured with a filter. The bottom curve was recorded with the 5-MHz filter.

The amplitude error results from the additional attenuation resulting from the scatter of the filter components.

Approx. 30 cycles were used for the averaged display. This corresponds to a measuring duration of approx. 1 minute.

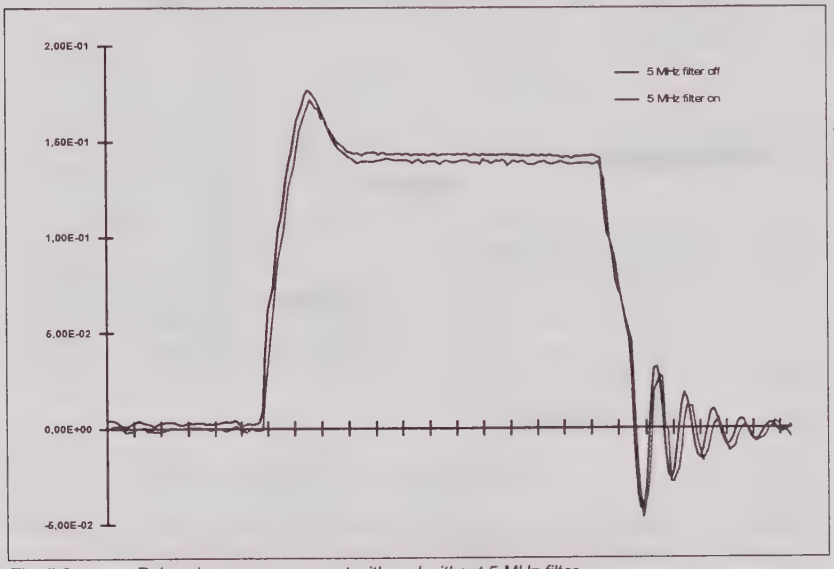


Fig. 5.6: Pulse shape measurement with and without 5 MHz filter

The internal amplifier offset is automatically measured and compensated at the start of the measurement. A best-fit procedure is started at the end of the measurement and if the tolerance mask is switched on. This procedure optimally fits the result in the tolerance mask. The pulse shape is displayed without modifications if the conformity cannot be achieved.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be pressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

The results are presented during the measurement in graphic form (see below). The displayed results are overwritten cyclically with each recording.

Results for the three different types of load are shown below.

a) 50 Ω

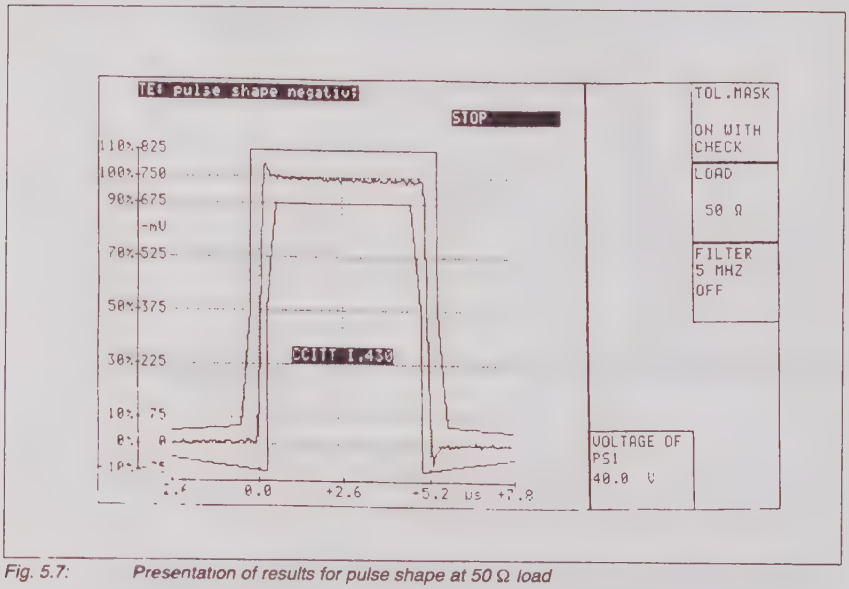


Fig. 5.7: Presentation of results for pulse shape at 50 Ω load

b) 5,6 Ω

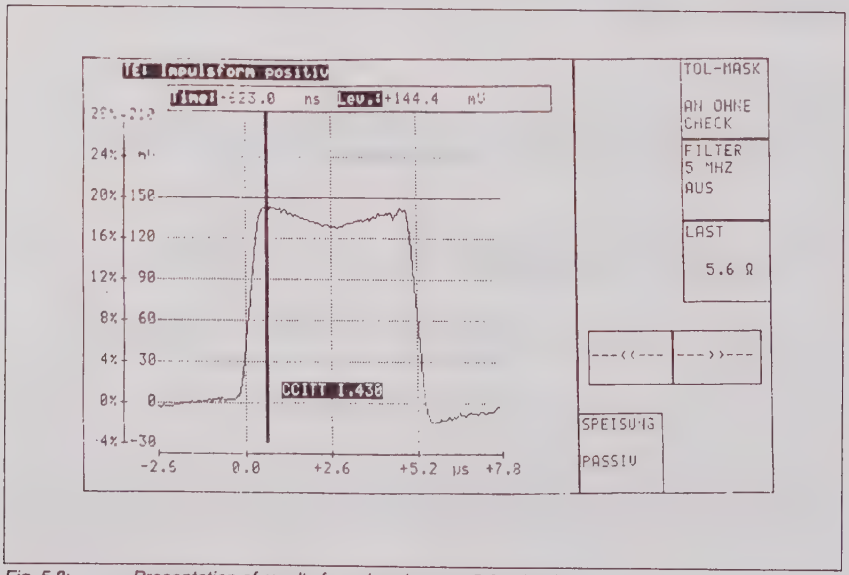


Fig. 5.8: Presentation of results for pulse shape at 5.6 Ω load

c) 400 Ω

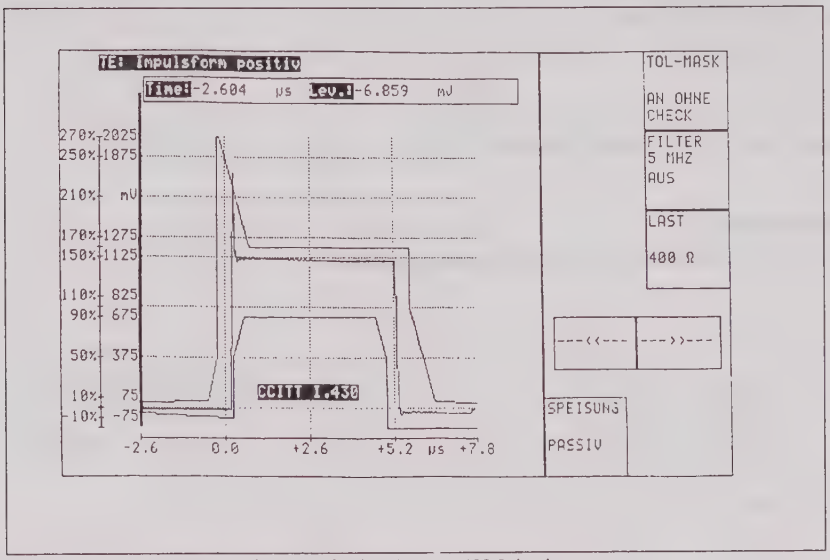


Fig. 5.9: Presentation of results of pulse shape at 400 Ω load

When TOL.MASK ON is set, a best-fit procedure is always carried out after STOP, in order to fit the measuring result optimally into the mask horizontally. The conformity statement is only made afterwards. This process occurs automatically.

A best-fit procedure is also carried out automatically after stop with the setting:

Load:	400 Ω
Tol. mask:	ON
Data processing:	MEAN VALUE

which fits the measuring result optimally into the tolerance mask vertically. The conformity statement is only made afterwards.

The RESULT key (T2) can be used to change to a "results mode" after the measurement has been terminated with T3. The results can now be indicated numerically point for point using a superimposed line cursor. The tolerance violations are indicated with a superimposed tolerance curve. "↑ NC" is used as the marking for violation of the upper tolerance mask and "↓ NC" for violation of the lower tolerance mask.

Measured values are displayed in the following form:

```
Time = +1.379 µs    Level = +725.7 mV
```

Time = t - $t_{TRIGGER}$

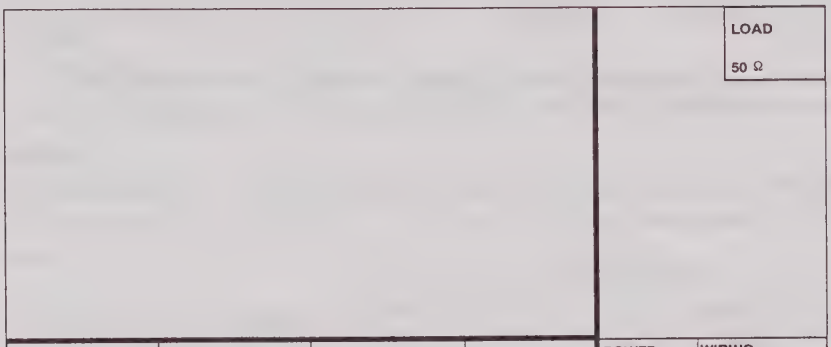
The cursor can be displaced roughly on the x-axis by touching the required time range (approx. ± 15 pixels). It is also possible to move pixel by pixel to the left or right with the two touch fields

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.1.4 Frame delay

(ETS §A.8.2.3)



Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
FRAME DELAY
CLOCK ACCURACY
IMPEDANCE OF ACTIVE TRANSMITTER
PULSE UNBALANCE
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY

TRANS. FRAME	CLOCK INTERNAL	LOAD	POWER FEEDING	WIRING CONFIG.
Binary "1"	INTERNAL	50 Ω	PASSIVE	FREE CONFIG.
Binary "0"	EXT: 5 Hz 0.5 Ulpp	100 Ω	NORMAL	CONFIG. 1
0AAH	EXT: 20 Hz 0.125 Ulpp		RESTRIC-TED	CONFIG. 2
$2^9 - 1$	EXT:50 Hz 0.05 Ulpp		EXTERNAL	CONFIG. 3a
$2^{11} - 1$	EXT: 2 kHz 0.05 Ulpp			CONFIG. 3b
$2^{13} - 1$	EXTERNAL 12.288 MHz			CONFIG. 4 (IDEAL)
$2^{15} - 1$				
$2^{17} - 1$				
$2^{19} - 1$				

The external clock settings with the superimposed jitter can be set using the **JITTER** option.

JITTER OPTION

All CCITT configurations are realised with the **ARTIFICIAL LINE** option.

ARTIFICIAL LINE OPTION

In order to prevent interferences from cancelling the effect, a jitter frequency of 2017 Hz is set in the case of "ext.2 kHz, 0.05UI_{pp}".

Dependencies

The following dependencies exist in this menu:

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24 V	24 V	-
-	32 V	32 V	-
-	42 V	42 V	-

Measured quantity

The frame delay of the TE is the time between the start of the transmitter frame and the start of the receiver frame. The permissible delay is [2 UI - 7 % UI] ... [2 UI + 15 % UI]

1 UI = 250 μs / 48 = 5,208 μs.

Test method

Test object TE is activated by INFO4 and transmits INFO3 (F7). The time between the F/L bit of the receiver and transmitter frames is measured by counting a reference clock.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

During the measurement, the result is displayed as shown below

`tmin = %`	minimum frame delay in % of one UI
`tmax = %`	maximum frame delay in % of one UI
`tavg = %`	average frame delay in % of one UI

The last measured value remains in the display after terminating the measurement or changing to RESULT. The message

```
AN2: L1 restricted active
```

is output if loss of the layer 1 connection is detected during the measurement. The measured values for t_{min} and t_{max} are regenerated for each measuring cycle. One measuring cycle includes approx. 10000 consecutive frames (and takes approx. 2.5 s). The mean frame delay is also calculated using this number of measured values.

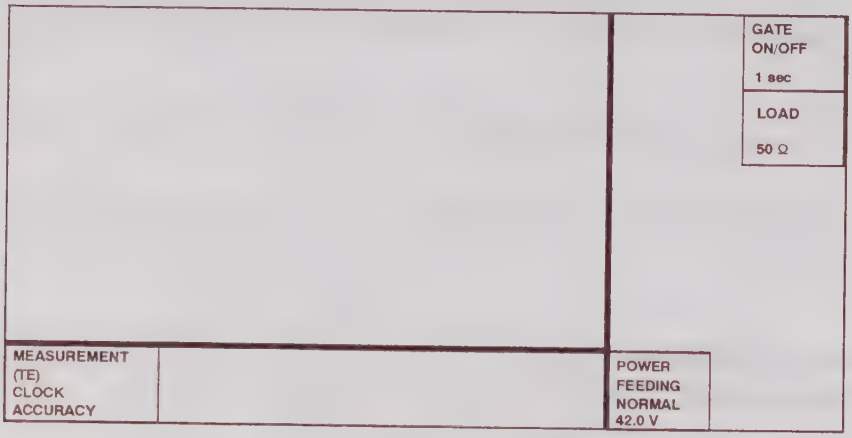
The conformity of the result is indicated by **C** (= CONFORM) or **NC** (= NOT CONFORM).

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.1.5 Clock accuracy

(ETS §A.8.1)



Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
FRAME DELAY
CLOCK ACCURACY
IMPEDANCE OF ACTIVE TRANSMITTER
PULSE UNBALANCE
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY

GATE ON/OFF	LOAD	POWER FEEDING
1 sec	50 Ω	PASSIVE
5 sec	100 Ω	NORMAL
		RESTRICTED
		EXTERNAL

Dependencies

The following dependencies exist in this menu:

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24 V	24 V	-
-	32 V	32 V	-
-	42 V	42 V	-

Measured quantity

This measuring mode is used to measure the accuracy of the TE activation signal INFO1.

Test method

The test object transmits INFO1, e.g. after the handset has been off-hook for a maximum of approx. 30 secs. A 384-kHz measuring clock is generated and measured in synchronism with this 24-kHz signal (+ 1, - 1, 0, 0, 0, 0, 0, 0). A 48-MHz oscillator functions as the basic clock for the selectable gate time of 1 sec and 5 secs.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

During the measurement, the result appears in the form

```
df/f = - 122 ppm
```

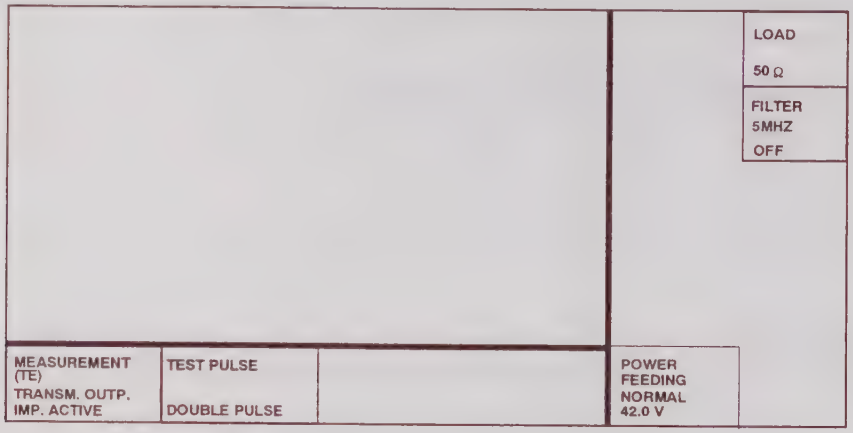
The last measured value remains in the display after terminating the measurement or changing to RESULT. The conformity of the result is indicated by **C** or **NC**.

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.1.6 Transmitter output impedance active

(ETS §A.8.5.1.2. Test B)



Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
FRAME DELAY
CLOCK ACCURACY
TRANSMITTER OUTPUT IMPEDANCE ACTIVE
PULSE UNBALANCE
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY

TEST PULSE	LOAD	FILTER 5 MHZ	POWER FEEDING
POSITIVE	50 Ω	OFF	PASSIVE
NEGATIVE	400 Ω	ON	NORMAL
DOUBLE PULSE			RESTRICTED
			EXTERNAL

Dependencies

The following dependencies exist in this menu:

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24 V	24 V	-
-	32 V	32 V	-
-	42 V	42 V	-

Measured quantity

The parameter is the internal resistance of the active TE transmitter (power up; activated; F7). The stimuli signal is the INFO4 which is sent by the K1403 to the test object.

Test method

The amplitude value for positive and negative pulses is measured (U+, U-). The transmitter is loaded with a load resistance of either R_L = 50 Ω ± 10 % or R_L = 400 Ω ± 10 %.

The measured value ($R_{NOM} \geq 20\ \Omega$) is calculated from:

$$R_{ACT} = \frac{U^+ - U^-}{\frac{U^-}{0{,}9 \cdot R_L} - \frac{U^+}{1{,}1 \cdot R_L}}$$

; U^+ at $0{,}9 * R_L$; U^- at $1.1 * R_L$

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

During the measurement, the result appears in the form

		Measurement with
R [+ -] =	Ω	Double pulse
R [-] =	Ω	Negative pulse and double pulse
R [+] =	Ω	Positive pulse and double pulse

The last measured value remains in the display after terminating the measurement or changing to RESULT.

Measuring accuracy

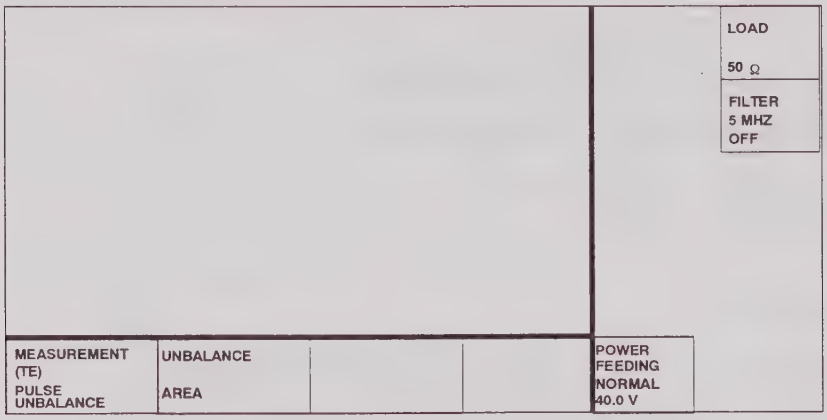
See *Appendix* "Technical data for electrical characteristics".

During the measurement with only positive or only negative pulses the test object must be able to produce isolated positive or negative pulses. Either all three measured values are specified (double pulse) or only the positive single pulse or only the negative single pulse depending on the test pulse selected.

In addition, at least two measurements must be waited for before a valid result is present. Both load resistors R_L ± 10 % must be measured before a valid result can be calculated. The results are constantly averaged exponentially to improve the accuracy. It is therefore recommendable to wait for a few cycles in order to achieve the full accuracy.

5.1.7 Impuls-Unsymmetrie

(ETS §A.8.5.4.1; §A.8.5.4.2)



Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
FRAME DELAY
CLOCK ACCURACY
IMPEDANCE OF ACTIVE TRANSMITTER
PULSE UNBALANCE
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY

TEST PULSE	POWER FEEDING	LOAD	FILTER 5 MHZ
AREA	PASSIVE	50 Ω	OFF
AMPLITUDE	NORMAL	100 Ω	ON
	RESTRICTED		
	EXTERNAL		

Dependencies

The following dependencies exist in this menu:

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24 V	24 V	-
-	32 V	32 V	-
-	42 V	42 V	-

Measured quantity

The difference in area between the positive and negative signal half-waves referred to the nominal pulse area is known as the pulse unbalance and is determined in [%].

The deviation of the pulse amplitude measured in the middle of a pulse with reference to the nominal amplitude of 750 mV is called pulse amplitude unbalance and is calculated in [%].

Test method

The pulse unbalance is formed by integration of the pulse areas. For this purpose the TE is activated via INFO4 (*B1,B2="1"*) and sends INFO3 (B1=B2="1"). The first double pulse of the INFO3 (F/L-bit) is acquired und integrated numerically. All measured values thus acquired are averaged exponentially over the measuring time and output.

In order to measure the amplitude pulse unbalance, the TE is activated via an INFO4 (B1,B2="0") and transmits INFO3 (B1,B2="0"; high density pattern), if a data loop or a test mode was switched on. The amplitude is recorded in the middle of each double pulse and the greatest deviation each relative to 750 mV is calculated for an entire frame. The measured values are averaged over the measuring time and output.

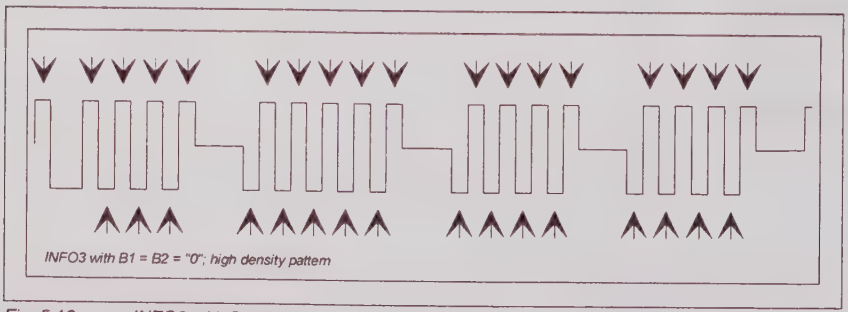


Fig. 5.10: INFO3 with B1=B2="0"

The results which are output are determined as described below.

a) Pulse area unbalance (surface integral)

$$\frac{\Delta F}{F_{nom}} = \frac{\Delta t \times \sum_{i=0}^{i=255} M_i}{F_{nom}}$$

M_i is the measured amplitude value in storage position " i"

$\Delta t \approx 64ns$ is the sampling step width

$$\left.\frac{\Delta F}{F_{nom}}\right|_{rel} = \frac{\Delta F}{F_{nom}} \times 100\%$$

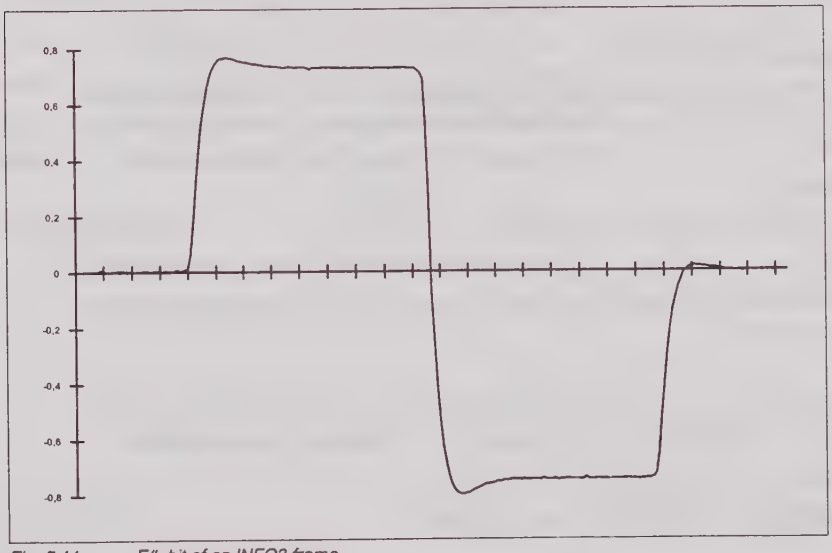


Fig. 5.11: F/L bit of an INFO3 frame

Each display point in the above curve represents a measured point which has been stored in one of 256 storage locations and measured in one of 256 successive frames (MPS - multi-period sampling method). As a result of the low capacitive coupling of the instrument amplifier, the DC offset at the beginning of the INFO3 frame is as low as if INFO0 had previously been received. Its influence on the measuring accuracy is thus very low.

b) Pulse amplitude unbalance

The pulse amplitude unbalance is calculated as follows.

$$\frac{\Delta U_{+}}{U_{nom}} = \frac{A_{x0}}{U_{nom}} \quad \left| \quad A_{x0}|_i = A_{x0}|_{i-1} + \frac{M_i - A_{x0}|_{i-1}}{K} \right.$$

$$\frac{\Delta U_{-}}{U_{nom}} = \frac{A_{x1}}{U_{nom}} \quad \left| \quad A_{x1}|_i = A_{x1}|_{i-1} + \frac{M_i - A_{x1}|_{i-1}}{K} \right.$$

The values of A_{X0} and A_{X1} are the exponential mean values (averaging constant K = 32) of the pulse amplitude at the center of the positive and negative half-waves respectively of a high density pattern. These mean values are continuously calculated during the measurement. The results are output relatively as a percentage.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

During the measurement of the pulse amplitude unbalance the receiving signal is checked. If an INFO3 with B1,B2="1" is detected, the following message appears

```
AN2: binary zeros ?
```

This means that no suitable INFO3 was detected.

Presentation of results (RESULT)

During the measurement *pulse area unbalance* the result is displayed as shown below

```
dF/Fnom = %
```

The last measured value remains in the display after terminating the measurement or changing to RESULT. Whether the area unbalance exceeds the limit value ± 5% or not is indicated by C or NC respectively after STOP.

During the measurement *pulse amplitude unbalance*, the result is displayed as follows

```
dU+/Unom = %
```

```
dU-/Unom = %
```

The last measured value remains in the display after terminating the measurement or changing to RESULT. Whether the amplitude unbalance exceeds the limit value ± 10% or not is indicated by **C** or **NC** respectively after STOP.

If during the measurement measured values larger than ± 25% are recognized, the mean value calculation is switched off and the current maximum values are output until they fall below the limit value again. This is necessary because it is possible that the test loop or the test mode in the test object are switched on only after the start of the measurement. Thus extreme measuring results may be displayed.

If a different B-channel content is set instead of a correct high density pattern, the following measuring results may be displayed:

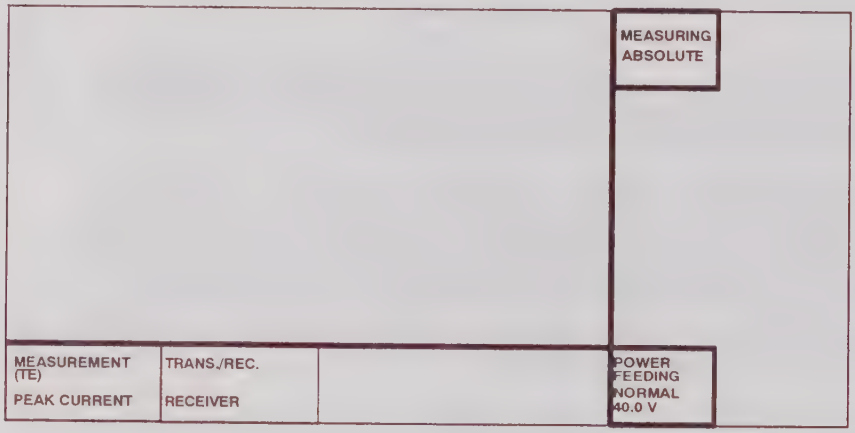
-100%	if a zero level occurs instead of a positive level
+100%	if a zero level occurs instead of a negative level
-200%	if a negative level occurs instead of a positive level
+200%	if a positive level occurs instead of a negative level

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.1.8 Peak current

(ETS §A.8.5.1.2 Test C&E; §A.8.6.1.1 Test B)



Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
FRAME DELAY
CLOCK ACCURACY
IMPEDANCE OF ACTIVE TRANSMITTER
PULSE UNBALANCE
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY

TRANS./REC.	MEASUREMENT	POWER FEEDING
RECEIVER	ABSOLUTE	PASSIVE
TRANSMITTER	RELATIVE	NORMAL
		RESTRICTED
		EXTERNAL

Dependencies

The following dependencies exist in this menu:

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24 V	24 V	-
-	32 V	32 V	-
-	42 V	42 V	-

Measured quantity

The peak current created by an applied test voltage is measured at the transmitter as well as at the receiver of the non-active test object. The current flows via the S_0 transmitter and the protective circuit of the test object.

Test method

The sinusoidal test voltage U_{pp} = 2.4 V (+ 0 % / - 4 %) is applied across the measuring panel to the TE and the resulting load-independent current recorded with a precision transformer. The peak current value is determined from a signal shape measurement.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

`INIT/START`

Before switching the test object, the closed-circuit current created due to the parasitic capacities of the K1403 is measured internally. The switchover to the test object occurs automatically as soon as the closed-circuit current has been recorded with sufficient accuracy.

The start of the measurement is indicated by

`MEASURE`

The basic current of the test set-up $I_{0,}$, i.e. the current which flows through the capacitive load components, can be determined during the measurement ABSOLUTE and subtracted from all subsequently measured values as an offset value. This is carried out each time the `ZERO BALANCE` key is pressed (impedance value of the reference Z_{ref} = 2 kΩ).

During the measurement RELATIVE, an externally switchable reference at the S_0 bus can be measured and I_{ref} used as reference value. This occurs every time the `600µA BALANCE` key ist pressed.

The START/STOP key must be depressed again to stop the measurement. The following appears

`STOP`

Presentation of results (RESULT)

During the measurement, the result appears in the form

`Is = +650.1µA`

or

`Is = -650.1µA`

The larger of the two current half-waves is output in each case with its sign. The last measured value remains in the display after terminating the measurement or changing to RESULT. Violation of the limits of ± 600 µA is indicated by **NC** following STOP; otherwise **C** appears.

The measuring results displayed are calculated as follows depending on the measurement selected:

$$I_{Absolute} = (I_{mes} - I_0) - I_C$$

$$I_{Relative} = \left(\frac{I_{mes}}{I_{ref}} \times 600\mu A\right) - I_C$$

I_0 = Offset Value

I_{ref} = Reference Value

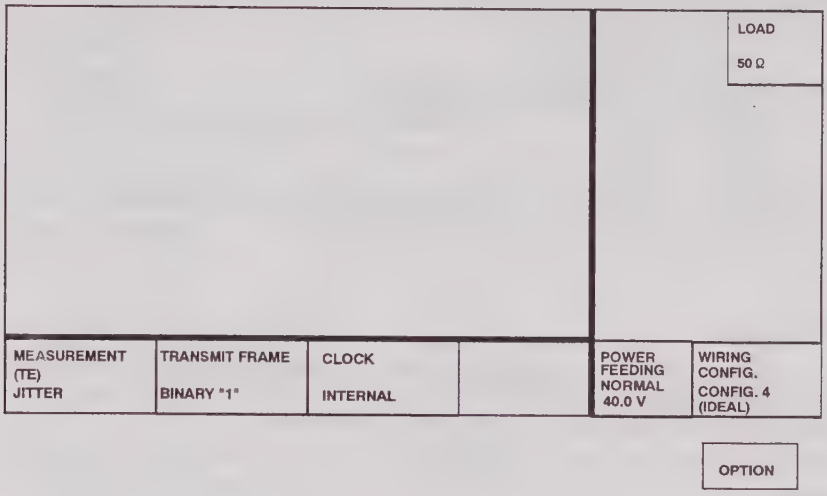
I_c = Basic Current K1403

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.1.9 Jitter

(ETS §A.8.2.2 Test A)



Setting parameters (MENU)

MEASUREMENT	TRANS. FRAME	CLOCK	LOAD	POWER FEEDING	WIRING CONFIG.
IMPEDANCE	Binary "1"	INTERNAL	50 Ω	PASSIVE	FREE CONFIG.
UNBALANCE	Binary "0"	EXTERNAL	100 Ω	NORMAL	CONFIG. 1
PULSE SHAPE	ALT. FRAME			RESTRICTED	CONFIG. 2
FRAME DELAY	$2^9 - 1$			EXTERNAL	CONFIG. 3a
CLOCK ACCURACY	$2^{11} - 1$				CONFIG. 3b
IMPEDANCE OF ACTIVE TRANSMITTER	$2^{13} - 1$				CONFIG. 4 (IDEAL)
PULSE UNBALANCE	$2^{15} - 1$				
PEAK CURRENT	$2^{17} - 1$				
JITTER	$2^{19} - 1$				
RECEIVER SENSITIVITY					

All CCITT configurations are realized via the **ARTIFICIAL LINE** option.

ARTIFICIAL LINE OPTION

Dependencies

The following dependencies exist in this menu:

POWER FEEDING			
PASSIVE	NORMAL	RESTRICTED	EXTERNAL
-	EDIT	EDIT	-
-	24 V	24 V	-
-	32 V	32 V	-
-	42 V	42 V	-

Measured quantity

The peak value of the phase fluctuations of the transmitter signal (INFO3) is recorded with the jitter measurement at the TE output. The full edges, i.e. those which pass through zero, must be evaluated for the measurement.

Test method

The test object is activated with INFO4 and transmits INFO3 (F7). Various selectable test patterns are transmitted in the INFO4 data channels (cf. setting parameters) in order to generate as many full edges as possible in the INFO3 by means of a loop in test object TE. Measurement is performed by counting the time which elapses from a full edge of the transmitted signal (192-kHz reference clock) to the corresponding edge of the INFO3 test signal.

This jitter mode is included in the performance of the basic K1403 unit. It differs from that offered with the JITTER option in that a counting method is used here and that no clock regain via the connected phase comparator and high-pass filter are available for the evaluation (see ETS test configuration for jitter test). The memory depth available for the counted values results in a smallest evaluated jitter frequency of 0.2 Hz with this method (binary "1" in the data channels) or of 1 Hz with binary "0" in the data channels.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

During the measurement, the result appears in the form

```
I(UI) = +5.20 %
```

The last measured value remains in the display after the measurement has been terminated or a change has been made to RESULT.

Measuring accuracy

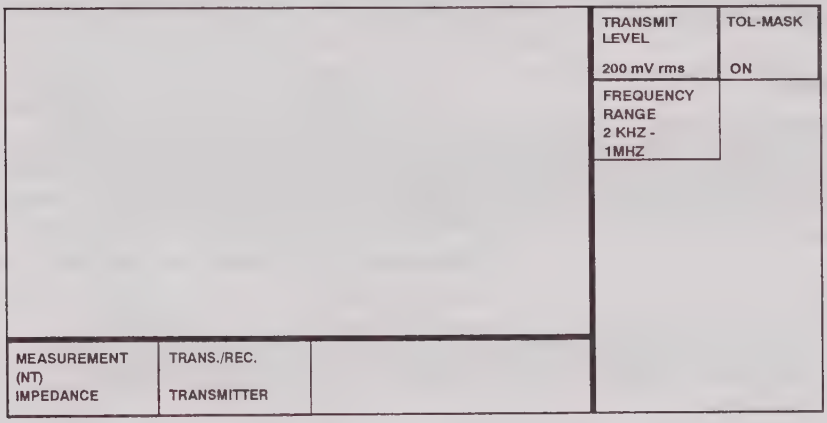
See *Appendix* "Technical data for electrical characteristics".

5.1.10 Receiver sensitivity

The measuring mode *Receiver Sensitivity* is described in detail in the operating manual Functional Tests for K1403.

5.2 Electrical measurements NT

5.2.1 Impedance



Setting parameters (MENU)

MEASUREMENT	TRANS./REC.	TRANSMIT LEVEL	TOL. MASK	FREQUENCY RANGE
IMPEDANCE	RECEIVER	EDIT	OFF	EDIT
UNBALANCE	TRANSMITTER	LAST EDIT VALUE	ON	LAST EDIT VALUE
PULSE SHAPE		CCITT	ON WITH CONF. TEST	2 kHZ-1 MHZ
IMPEDANCE OF ACTIVE TRANSMITTER		100 mV rms		2 kHZ-40 kHZ
PEAK CURRENT		200 mV rms		10 kHZ-200 kHZ
JITTER		300 mV rms		50 kHZ-1 MHZ
RECEIVER SENSITIVITY		400 mV rms		
FRAME COMPATIBILITY		500 mV rms		

Measured quantity

The parameter is the frequency-related magnitude of the impedance of the NT receiver or the passive transmitter (transmitted signal "INFO 0"). The test object is in the deactivated status (G1).

Test method

A sinusoidal test voltage is applied to the test object. The current in the test circuit is measured for different test frequencies between 2 kHz and 1 MHz. Measurement is performed relative to a reference resistance (200 Ω). All the effects of thermal drift or internal frequency dependencies are minimized through calibration and reference measurements.

The reference measurement is currently run before the first measurement and then only if setting parameters have been changed and the measurement restarted or when there is a new start after a calibrating measurement.

Starting from mid 1996 a new board ANALOG1 is in use. With its release version C73249-A11-L80, the reference measurement is run prior to each measurement. Further more no calibration steps for the transmitter and receiver are necessary anymore.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG1 are initialized. The following status message appears in the display

```
INIT/START
```

Transmitter and receiver calibration is then performed automatically for the first measurement performed each time the unit is switched on and at intervals of approx. 10 minutes thereafter. Automatic calibration takes approx. 20 s and is acknowledged by the two status messages

```
CALIBR.SEND
```

```
CALIBR.REC
```

After each measurement START, a reference measurement is first performed for the relative measurement. This takes approx. 15 s and is indicated by the following message.

```
REFERENCE
```

The start of the measurement itself is indicated by

```
MEASURE
```

A complete test cycle in the selected frequency range, including all calculations, evaluations and graphic output on the display, requires approximately $t_{MEAS} \approx 15$ s.

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

The results are presented during the measurement in graphic form. The displayed results are overwritten cyclically each time the frequency range is run through, the current test point being indicated by a continuous bar cursor.

The axes are inscribed in accordance with the selected parameters. A double logarithmic inscription and presentation are used.

The RESULT key (T2) can be used to change to a "results mode" after the measurement has been terminated with T3. The results can now be indicated numerically point for point using a superimposed line cursor. The tolerance violations are indicated with a superimposed tolerance curve (marked 'NC').

Measured values are indicated in the following form

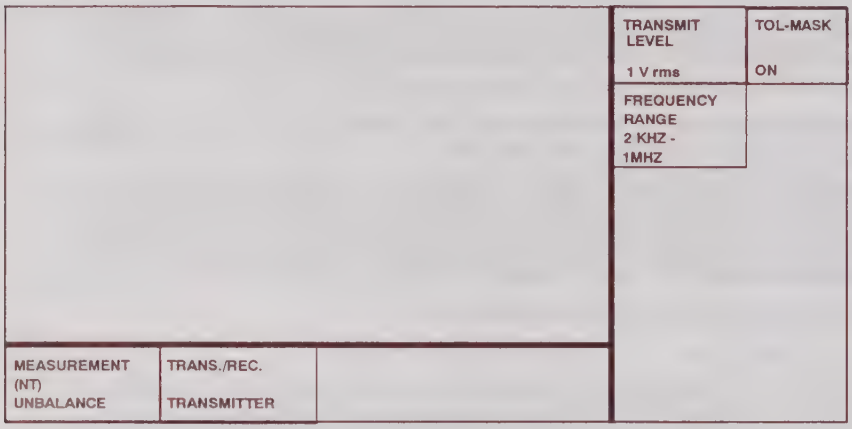
```
Frequ.: 3.450  kHz      Imped.: 2.244   kΩ
```

The cursor can be displaced roughly on the x-axis by touching the required frequency range (approx. ± 15 pixels). It is also possible to move pixel by pixel to the left or right with the two touch fields

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.2.2 Unbalance



Setting parameters (MENU)

MEASUREMENT	TRANS./REC.	TRANSMIT LEVEL	TOL. MASK	FREQUENCY RANGE
IMPEDANCE	RECEIVER	EDIT	OFF	EDIT
UNBALANCE	TRANSMITTER	LAST EDIT VALUE	ON	LAST EDIT VALUE
PULSE SHAPE		CCITT	ON WITH CONF. TEST	2 kHZ-1 MHZ
IMPEDANCE OF ACTIVE TRANSMITTER		1 V rms		80 kHZ-1 MHZ
PEAK CURRENT		0.9 V rms		
JITTER		0.8 V rms		
RECEIVER SENSITIVITY		0.7 V rms		
FRAME COMPATIBILITY				

Measured quantity

The frequency-related unbalance against the protective earth (longitudinal conversion loss LCL) is measured at the NT input and NT output. The test object is in the deactivated status G1.

Test method

A sinusoidal test voltage is applied to the test object. The voltage VT at the output or input of the test object is measured relative to the test voltage VP for various test frequencies between 2 kHz and 1 MHz (LCL). Measurement is performed relative to a reference unbalance. All effects of thermal drift or internal frequency dependencies are minimized with calibration and reference measurements.

$$a_{LCL} = 20 \cdot \log \frac{|U_P|}{|U_T|} dB$$

The reference measurement is currently run before the first measurement and then only if setting parameters have been changed and the measurement restarted or when there is a new start after a calibrating measurement.

Starting from mid 1996 a new board ANALOG1 is in use. With its release version C73249-A11-L80, the reference measurement is run prior to each measurement. Further more no calibration steps for the transmitter and receiver are necessary anymore.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG1 are initialized. The following status message appears in the display

`INIT/START`

Transmitter and receiver calibration is then performed automatically for the first measurement performed each time the unit is switched on and at intervals of approx. 10 minutes thereafter. Automatic calibration takes approx. 20 s and is acknowledged by the two status messages

`CALIBR.SEND`

`CALIBR.REC`

After each measurement START, a reference measurement is first performed for the relative measurement. This takes approx. 10 s and is indicated by the following message.

`REFERENCE`

The start of the measurement itself is indicated by

`MEASURE`

A complete test cycle in the selected frequency range, including all calculations, evaluations and graphic output on the display, requires approximately $t_{MEAS} \approx 10$ s.

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

The results are presented during the measurement in graphic form. The displayed results are overwritten cyclically each time the frequency range is run through, the current test point being indicated by a continuous cursor at the bottom of the screen.

The axes are inscribed in accordance with the selected parameters. A double logarithmic inscription and presentation are used.

The RESULT key (T2) can be used to change to a "results mode" after the measurement has been terminated with T3. The results can now be indicated numerically point for point using a superimposed line cursor. The tolerance violations are indicated with a superimposed tolerance curve (marked 'NC'). Measured values are indicated in the following form

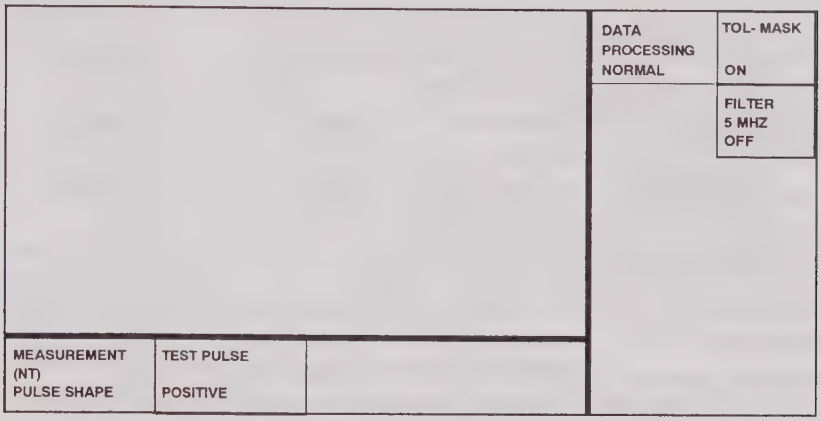
```
Frequ.: 2.88  kHz  Imped.: 71.2   dB
```

The cursor can be displaced roughly on the x-axis by touching the required frequency range (approx. ± 15 pixels). It is also possible to move pixel by pixel to the left or right with the two touch fields

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.2.3 Pulse shape



Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
IMPEDANCE OF ACTIVE TRANSMITTER
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY
FRAME COMPATIBILITY

TEST PULSE	DATA PROCESSING	TOL. MASK	FILTER 5 MHZ
POSITIVE	NORMAL	OFF	OFF
NEGATIVE	MAX. VALUES	ON	ON
	MIN. VALUES		
	MEAN VALUE		

Dependencies

TOL. MASK	
OFF	ON
-	DATA PROCESSING
(NORMAL)	NORMAL
-	MAX. VALUES
-	MIN. VALUES
-	MEAN VALUE

Measured quantity

When measuring pulse shape, the shape of the NT transmitter signal is recorded. It is possible here to record either an individual positive or negative pulse. A 50-Ω resistor is used as a fixed terminator.

Test method

The network terminator NT is brought to the status (G1 I1 received) by INFO1 and transmits INFO2. The change to the status (G3 active) is then initiated by INFO3. The change from G1 to G3 requires a transition time of several seconds since an analog PLL in the K1403 responds in addition. The inherent jitter of the test module is suppressed by this ($\varphi_{remainder}$ ~ 40 ns). This procedure requires several seconds (5 to 30 s) only when first activating the device after switch-on, after measurements on TE or of peak currents. In the case of all further activations after START/STOP, the process is completed within approx. 1 second. In the active status of the test object, this sends INFO4. The single pulses contained therein are automatically searched for at the start of the measurement. It is advantageous to transmit binary "1"s (zero level) in the B-channels of the test object.

A trigger window is activated by masking the required pulse (hardware). A total of 256 test points are recorded in this trigger window (MPS method, multi-periodic sampling). The trigger mask is shifted during the search procedure referred to above until the trigger condition (low, high, low level) is satisfied. The following message is output in the display during the search and if a single pulse cannot be found:

```
AN2: NO TRIGGER
```

The following can be selected for data processing

- Normal — Unmodified display of pulse shape
- Maximum value — Only display of largest amplitude values per position on the x-axis
- Minimum value — Only display of the smallest amplitude values per position on the x-axis
- Mean value — Only display of exponential mean value of all measured values per position on the x-axis

The hold function for minimum or maximum values can also store peaks which are non-recurring and also infrequent to enable the examination for tolerance violations. The mean function enables increasingly precise determination of the measured value per position on the axis as the measuring period proceeds. The exponential mean value simulates the function of a 1st order low-pass filter.

The exponential mean value is calculated according to the following equation

$$M_n = M_{n-1} + \frac{P_n - M_{n-1}}{K}$$

where: M_n = current mean value; $n \in N_0$

P_n = current measured value

K = averaging constant; K = 32

The advantage of this method is that a filter can be implemented without bandwidth losses. The calculation time required slows down the measuring cycle, however.

The effects of the three types of data processing is described in examples in section 5.1.3. measuring mode "pulse shape TE". A reduction in the noise level can also be achieved at the same speed but with a reduced bandwidth (5 MHz) using the selectable 3rd order low-pass filter. The accuracy of the amplitude is reduced to ± 2 %, however.

The internal amplifier offset is automatically measured and compensated at the start of the measurement. A best-fit procedure is started at the end of the measurement and if the tolerance mask is switched on. This procedure optimally fits the result in the tolerance mask. The pulse shape is displayed without modifications if the conformity cannot be achieved.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

The results are presented during the measurement in graphic form (see below). The displayed results are overwritten cyclically with each recording.

Typical results are shown in section 5.1.3., measuring mode "pulse shape TE". The results are presented in the same manner for the NT.

The RESULT key (T2) can be used to change to a "results mode" after the measurement has been terminated with T3. The results can now be indicated numerically point for point using a superimposed line cursor. The tolerance violations are indicated with a superimposed tolerance curve. "↑NC" is used as the marking for violation of the upper tolerance mark and "↓NC" for violation of the lower tolerance mark.

Measured values are indicated in the following form

```
Time = 2.62 µs      Level = -7.12 mV
```

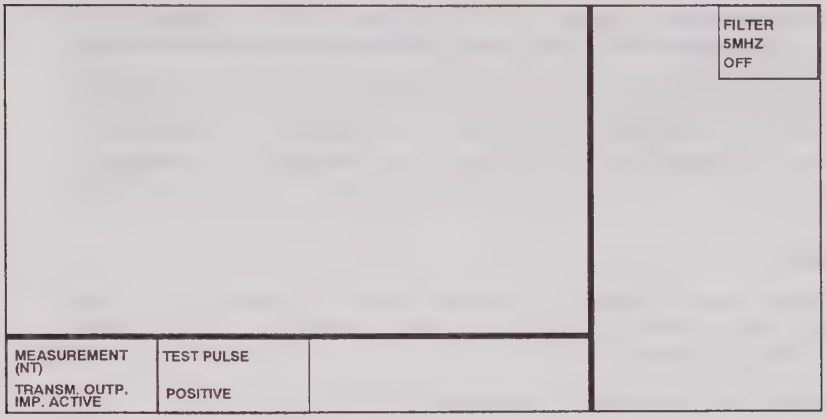
Time = t - $t_{TRIGGER}$

The cursor can be displaced roughly on the x-axis by touching the required frequency range (approx. ± 15 pixels). It is also possible to move pixel by pixel to the left or right with the two touch fields

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.2.4 Transmitter Output Impedance active



Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
TRANSMITTER OUTPUT IMPEDANCE ACTIVE
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY
FRAME COMPATIBILITY

TEST PULSE	FILTER 5 MHZ
POSITIVE	OFF
NEGATIVE	ON

Measured quantity

The parameter is the internal resistance of the active NT transmitter (G3; activated). The network terminator NT is brought to the status (G1 I1 received) by INFO1 and transmits INFO2. The change to the status (G3 active) is then initiated by INFO3. The change from G1 to G3 requires a transition time of several seconds since an analog PLL in the K1403 responds in addition. The inherent jitter of the test module is suppressed by this ($\varphi_{remainder}$ ≈ 40 ns). In the active status of the test object, this sends INFO4.

Test method

The amplitude value for positive and negative pulses is measured (U+, U-). The transmitter is loaded with a load resistance of either R_L=50Ω ±10% or R_L=400Ω ±10 %.

The measured value (R_{NOM} ≥ 20 Ω) is calculated from:

$$R_{ACT} = \frac{U^+ - U^-}{\frac{U^-}{0,9 \cdot R_L} - \frac{U^+}{1,1 \cdot R_L}}$$

; U^+ at 0,9 * R_L; U^- at 1.1 * R_L

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

During the measurement, the result appears in the form

	Measurement with
R [+ -] = Ω	(Double pulse; TE only)
R [-] = Ω	Negative pulse (and double pulse; TE only)
R [+] = Ω	Positive pulse (and double pulse; TE only)

The last measured value remains in the display after the measurement has been terminated or a change has been made to RESULT.

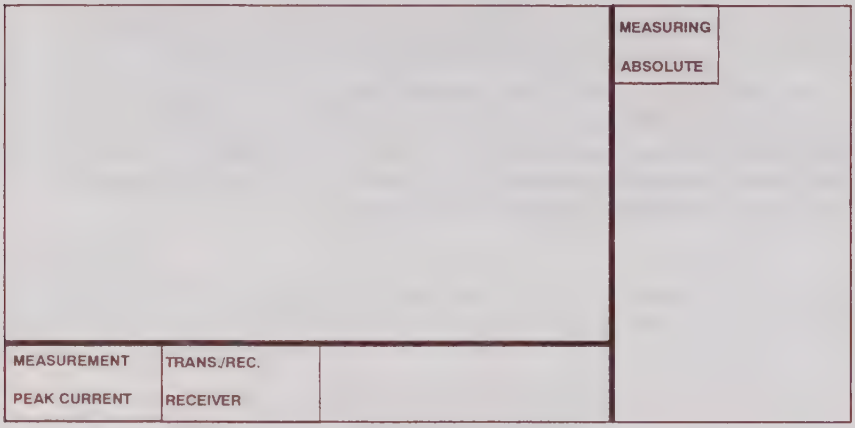
Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

The test object must be able to produce isolated positive or negative pulses. It is therefore advantageous to transmit binary "1"s in the B-channels.

In addition, at least two measurements must be waited for before a valid result is present. Both load resistors R_L ± 10 % must be measured before a valid result can be calculated. The results are constantly averaged exponentially to improve the accuracy. It is therefore recommendable to wait for a few cycles in order to achieve the full accuracy.

5.2.5 Peak current



Setting parameters (MENU)

MEASUREMENT
IMPEDANCE
UNBALANCE
PULSE SHAPE
IMPEDANCE OF ACTIVE TRANSMITTER
PEAK CURRENT
JITTER
RECEIVER SENSITIVITY
FRAME COMPATIBILITY

TRANS./REC.	MEASURING
RECEIVER	ABSOLUTE
TRANSMITTER	RELATIVE

Measured quantity

The peak current produced by the applied test voltage is measured both at the transmitter and at the receiver of the inactive test object NT. The current flows via the S_0 transmitter and the protective circuits of the test object.

Test method

The sinusoidal test voltage U_{pp} = 2.4 V (+0 % / -4 %) is applied to the NT across the measuring panel and the resulting load-independent current recorded with a precision transformer. The peak current value is determined from a signal shape measurement.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

`INIT/START`

Before switching the test object, the closed-circuit current created due to the parasitic capacities of the K1403 is measured internally. The switchover to the test object occurs automatically as soon as the closed-circuit current has been recorded with sufficient accuracy.

The start of the measurement is indicated by

`MEASURE`

During the measurement ABSOLUTE the basic current of the test set-up, i.e. the current which flows through the capacitive load components even when a test object is not connected, can be determined during the measurement and subtracted from all subsequently measured values as an Offset value. This is carried out each time the `ZERO BALANCE` key is pressed.

During the measurement RELATIVE an externally switchable reference at the S_0 bus can be measured and I_{ref} used as reference value. This occurs every time the `500µA BALANCE` key ist pressed (impedance of the reference Z_{ref} = 2.4 kΩ)

The START/STOP key must be depressed again to stop the measurement. The following appears

`STOP`

Presentation of results (RESULT)

During the measurement, the result appears in the form

```
Is = +650.1 µA
```

or

```
Is = -650.1 µA
```

The larger of the two current half-waves is output in each case with its sign. The last measured value remains in the display after the measurement has been terminated or a change has been made to RESULT. Violation of the limits of ±500µA is indicated by **NC** following STOP; otherwise **C** appears.

The measuring results displayed are calculated as follows depending on the measurement selected:

$$I_{Absolute} = (I_{mes} - I_0) - I_C$$

$$I_{Relative} = \left(\frac{I_{mes}}{I_{ref}} \times 500\mu A\right) - I_C$$

I_0 = OffsetValue

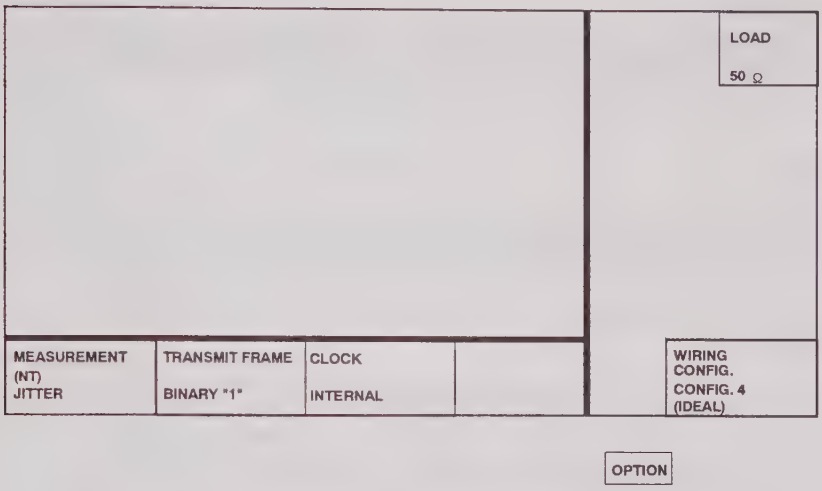
I_{ref} = ReferenceValue

I_c = BasicCurrent K1403

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.2.6 Jitter



Setting parameters (MENU)

MEASUREMENT	TRANSMIT FRAME	CLOCK	LOAD	WIRING CONFIG.
IMPEDANCE	Binary "1"	INTERNAL	50 Ω	FREE CONFIG.
UNBALANCE	Binary "0"	EXTERNAL	100 Ω	CONFIG. 1
PULSE SHAPE	ALT. FRAMES			CONFIG. 2
IMPEDANCE OF ACTIVE TRANSMITTER	$2^9 - 1$			CONFIG. 3a
PEAK CURRENT	$2^{11} - 1$			CONFIG. 3b
JITTER	$2^{13} - 1$			CONFIG. 4 (IDEAL)
RECEIVER SENSITIVITY	$2^{15} - 1$			
FRAME COMPATIBILITY	$2^{17} - 1$			
	$2^{19} - 1$			

All CCITT configurations are realized via the **ARTIFICIAL LINE** option.

ARTIFICIAL LINE OPTION

Measured quantity

The peak value of the phase fluctuations of the transmitter signal (INFO4) is recorded with the jitter measurement at the NT output. The full edges, i.e. those which pass through zero, must be evaluated for the measurement.

Test method

The network terminator NT is brought to the status (G1 I1 received) by INFO1 and transmits INFO2. The change to the status (G3 active) is then initiated by INFO3. The change from G1 to G3 requires a transition time of several seconds since an analog PLL in the K1403 responds in addition. The inherent jitter of the test module is suppressed by this ($\varphi_{remainder}$ ≈ 40 ns). In the active status of the test object, this sends INFO4.

Various selectable test patterns are transmitted in the INFO3 data channels (cf. setting parameters) in order to generate as many full edges as possible in the INFO4 by means of a loop in test object NT. Measurement is performed by counting the time which elapses from a full edge of the transmitter signal (192-kHz reference clock) to the corresponding edge of the INFO4 test signal.

This jitter mode is included in the performance of the basic K1403 unit. It differs from that offered with the JITTER option in that a counting method is used here and that no high-pass or low-pass filters are available for the evaluation. The memory depth available for the counted values results in a smallest evaluated jitter frequency of 0.2 Hz with this method (binary "1" in the data channels) or of 1 Hz with binary "0" in the data channels.

The value of the remaining jitter is superimposed on the result. Thus approx. 0.4 to 0.8 % UI jitter amplitude is present in the result which is generated by the test setup itself.

Measurement (START/STOP)

START/STOP key T3 is used to start the measurement. Firstly, the measuring panel and the module ANALOG2 are initialized. The following status message appears in the display

```
INIT/START
```

The start of the measurement is indicated by

```
MEASURE
```

The START/STOP key must be depressed again to stop the measurement. The following appears

```
STOP
```

Presentation of results (RESULT)

During the measurement, the result is displayed as follows

```
I(UI)        =   3.20 %
```

The last measured value remains in the display after terminating the measurement or changing to RESULT.

Measuring accuracy

See *Appendix* "Technical data for electrical characteristics".

5.2.7 Receiver sensitivity

The measuring mode *Receiver Sensitivity* is described in detail in the operating manual Functional Tests for K1403.

5.2.8 Frame compatibility

The measuring mode *frame compatibility* is described in detail in the operating manual Functional Tests for K1403.

6 Appendix

Technical data for the electrical characteristics can be found on the next few pages.

6.1 Technical data

6.1.1 Electrical characteristics

Impedance

General data for transmitter:

Signal shape	Sinusoidal
Frequency range	2 kHz to 1 MHz
Frequency resolution	1 Hz
Frequency setting accuracy	± 2 Hz
Transmitted signal amplitude	U_{rms} = 100 mV to 300 mV
Transmit level accuracy	± 5 % of measured value
Output impedance	< 20 Ω

General data for receiver:

Frequency range	2 kHz to 1 MHz
Level resolution	12 bits
Receiver bandwidth	< 25 Hz

Output/input impedance:

Measured value indication	Level of impedance in curve form as a function of frequency
Frequency setting range	a) 2 kHz to 1 MHz b) 2 kHz to 40 kHz c) 10 kHz to 200 kHz d) 50 kHz to 1 MHz
Measuring range	100 Ω to 5 kΩ
Measuring error	< 5 % of measured value for 2 kHz ≤ f ≤ 300 kHz < 7 % of measured value for f > 300 kHz
Tolerance system	Fade-in as per CCITT I.430

Impedance of the active transmitter

Measured value display	Internal impedance of the active transmitter when transmitting binary "0".
Measuring range	15 Ω to 25 Ω
Measuring error	± 2 Ω

Unbalance

General data	
Transmitted signal amplitude	700 mV to 1000 mV otherwise as for impedance measurement
Measured value display	Unbalance attenuation in curve form dependent on frequency
Frequency setting range	a) 2 kHz to 1 MHz b) 80 kHz to 1 MHz
Measuring range	38 dB to 78 dB
Insertion loss	2 kHz to 106 kHz a_e = 0.2 dB ±0.1 dB 106 kHz to 1 MHz a_e = 0.4 dB ±0.3 dB
Intrinsic unbalance	Up to 300 kHz > 74 dB, otherwise declining at 20 dB/dec
Measuring error	± 0.5dB of the measured value plus the intrinsic unbalance error
Tolerance system	Fade-in as per CCITT I.430

Transmitted signal pulse symmetry

Measured value display	a) numerical indication of the area unbalance b) amplitude unbalance of the 1st and 2nd double pulses
Measuring range	0 % to ± 10 %
Measuring error	a) Area ± 2.5 % b) Amplitude ± 2 %

Transmitted signal pulse shape

Measured value display	Graphic display of pulse shape dependent on time		
Input impedances	a) 5.6 Ω	± 0.16 Ω	
	b) 50 Ω	± 0.5 Ω	
	c) 400 Ω	± 4 Ω	
Measuring range, single pulse	a) -30 mV to	+210 mV at	5.6Ω
	b) -75 mV to	+825 mV at	50Ω
	c) -75 mV to	+2025 mV at	400Ω
Measuring range, double pulse	a) -225 mV to	+225 mV at	5.6Ω
	b) -825 mV to	+825 mV at	50Ω
	c) -2025 mV to	+2025 mV at	400Ω
Measuring error	a) ± 15 mV		
	b) ± 15 mV		
	c) ± 20 mV		
Level resolution	11 bits plus sign		
Time resolution	Double pulse = 3 * UI ÷ 256 ≙ 0.01 UI ≙ 62.5 ns Single pulse = 2 * UI ÷ 256 ≙ 0.008 UI ≙ 41.7 ns		

Peak current

Measured value display	Numerical display of peak current value
Transmitted frequency	96 kHz, sinusoidal
Transmitted amplitude	Upp = 2.4 V [+ 0 % / - 4%]
Measuring range	0.1 mA to 1 mA
Measuring error	± 30μA for i ≤ 600 μA ± 5 % of the measured value for i > 600 μA

Jitter (digital measuring mode in electrical characteristics menu)

Measured value display	Numerical display of jitter amplitude
Transmitted pattern	a) Binary "0" b) Binary "1" c) Alternating pattern "1"/"0AAhex", each in 40 frames d) PN pattern 2^9-1 e) PN pattern 2^{11}-1 f) PN pattern 2^{13}-1 g) PN pattern 2^{15}-1 h) PN pattern 2^{17}-1 i) PN pattern 2^{19}-1
Resolution	0.004 UI = 0.4 % UI
Resolution of display	In steps of 0.4% UI
Measuring range	0 to 0.5 UI = 50 % UI
Measuring error	a) TE 0.4 % UI b) NT 0.4 % UI + 2 % UI [self jitter]

Clock accuracy

Measured value display	Numerical display of frequency deviation
Measuring range	-200 ppm to +200 ppm
Measuring error	< 10 ppm
Measuring period	1 s, 5 s

Frame delay

Measured value display	Storing and numerical display of the min. and max. frame delay of a TE as well as continuous measured value output
Transmitted pattern	a) Binary "0" b) Binary "1" c) Alternating pattern "1"/"0AAhex", each in 40 frames d) PN pattern 2^9-1 e) PN pattern 2^{11}-1 f) PN pattern 2^{13}-1 g) PN pattern 2^{15}-1 h) PN pattern 2^{17}-1 i) PN pattern 2^{19}-1
Measuring range	± 1 UI = ± 100 % UI
Resolution	0.004 UI = 0.4 % UI
Resolution of display	In steps of 0.4% UI
Measuring error	0.006 UI = 0.6 % UI